

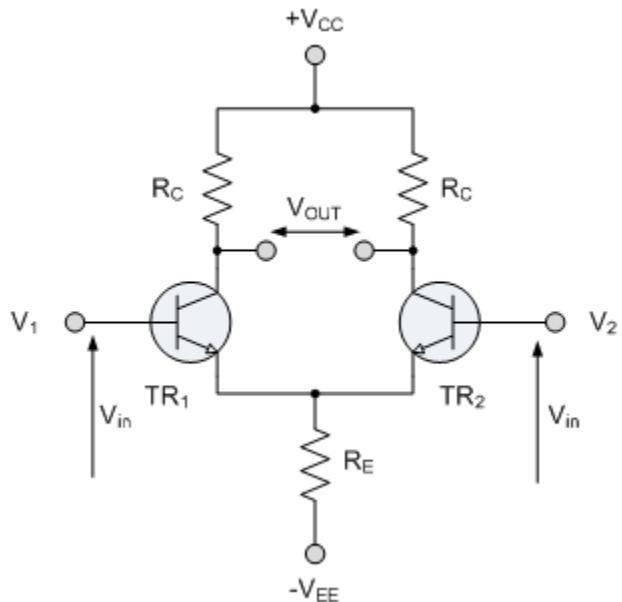
Operational Amplifiers (Supplementary note)

Ideal Operational Amplifier

As well as resistors and capacitors, **Operational Amplifiers**, or **Op-amps** as they are more commonly called, are one of the basic building blocks of Analogue Electronic Circuits. It is a linear device that has all the properties required for nearly ideal DC amplification and is used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation. An ideal operational amplifier is basically a 3-terminal device that consists of two high impedance inputs, one an **Inverting input** marked with a negative sign, ("-") and the other a **Non-inverting input** marked with a positive plus sign ("+").

The amplified output signal of an Operational Amplifier is the difference between the two signals being applied to the two inputs. In other words the output signal is a *differential* signal between the two inputs and the input stage of an Operational Amplifier is in fact a differential amplifier as shown below.

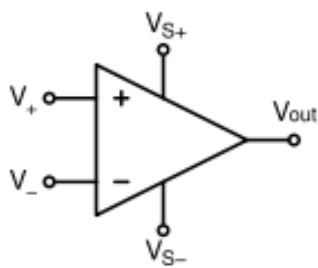
Differential Amplifier



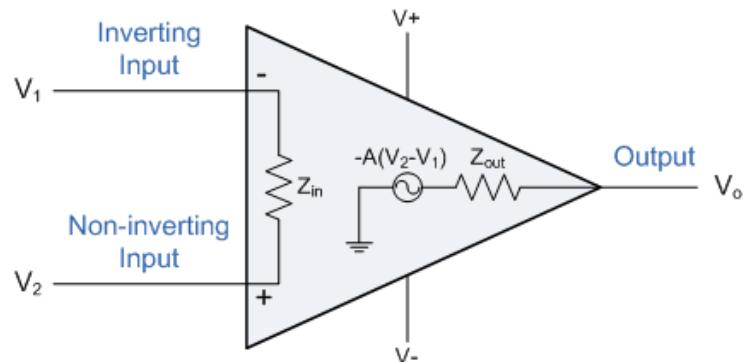
The circuit shows a generalized form of a differential amplifier with two inputs marked V_1 and V_2 . The two identical transistors TR₁ and TR₂ are both biased at the same operating point with their emitters connected together and returned to the common rail, $-V_{EE}$ by way of resistor R_E . The circuit operates from a dual supply $+V_{CC}$ and $-V_{EE}$ which ensures a constant supply. As the two base inputs are out of phase with each other, the output voltage, V_{OUT} , is the difference between the two input signals. So, as the forward bias of transistor TR₁ is increased, the forward bias of transistor TR₂ is reduced and vice versa. Then if the two transistors are perfectly matched, the current flowing through the common emitter resistor, R_E will remain constant.

Ideal Operational Amplifiers have an output of low impedance that is referenced to a common ground terminal and it should ignore any common mode signals. That means, if identical signals are applied to both the inverting and non-inverting inputs there should be no change at the output. However, in real amplifiers there is always some variation and the ratio of the change to the output voltage with regards to the change in the common mode input voltage is called the **Common Mode Rejection Ratio** or **CMRR**.

Operational Amplifiers have a very high open loop DC gain, commonly known as the **Open Loop Differential Gain**, and is given the symbol (A_o). By applying some form of **Negative Feedback** we can produce an operational amplifier circuit with a very precise gain characteristic that is dependent only on the feedback used. An operational amplifier only responds to the difference between the voltages at its two input terminals, known commonly as the "*Differential Input Voltage*" and not to their common potential. Then if the same voltage potential is applied to both terminals the resultant output will be zero.



Symbol of OpAmp



Equivalent Circuit for Ideal OpAmp

Idealized Characteristics

PARAMETER

Voltage Gain, (A)

IDEALIZED CHARACTERISTIC

Infinite - The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better, so for an ideal amplifier the gain will be infinite.

Input impedance, (Z_{in})

Infinite - Input impedance is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry.

Output impedance, (Z_{out})

Zero - The output impedance of the ideal operational amplifier is assumed to be zero so that it can supply as much current as necessary to the load.

Bandwidth, (BW)

Infinite - An ideal operational amplifier has an infinite Frequency Response and can amplify any frequency signal so it is assumed to have an infinite bandwidth.

Offset Voltage, (V_{io})

Zero - The amplifiers output will be zero when the voltage difference between the inverting and non-inverting inputs is zero.

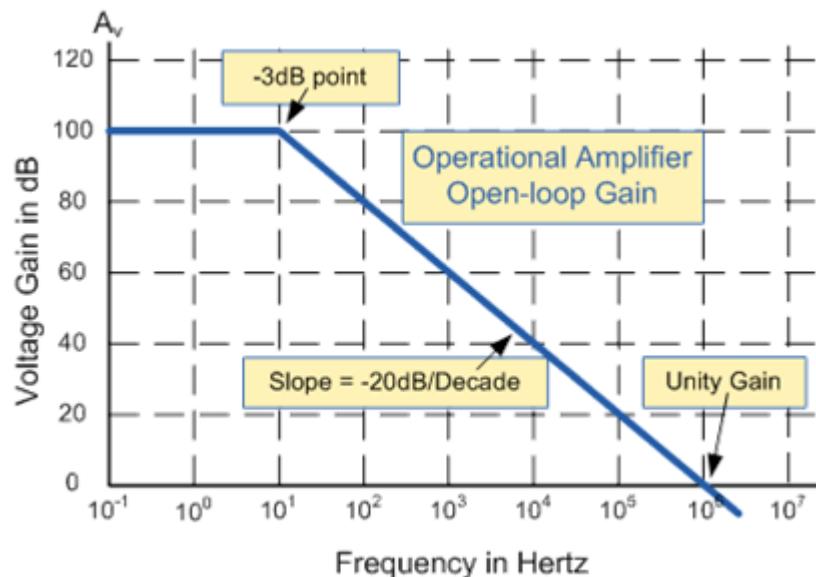
It is important to remember two properties known as the **golden rules**, as they help understand the working of the amplifier with regards to analysis and design of operational amplifier circuits.

1. **No current flows into either input terminal** (the current rule)
2. **The differential input offset voltage is zero** (the voltage rule).

However, real **Operational Amplifiers** (e.g. 741) do not have infinite gain or bandwidth but have a typical "Open Loop Gain" which is defined as the amplifiers output amplification without any external feedback signals connected to it and for a typical operational amplifier is about 100dB at DC (zero Hz). This output gain decreases linearly with frequency down to "Unity Gain" or 1, at about 1MHz and this is shown in the following open loop gain response curve. From this frequency response curve we can see that the product of the gain against frequency is constant at any point along the curve. Also that the unity gain (0dB) frequency also determines the gain of the amplifier at any point along the curve. This constant is generally known as the **Gain Bandwidth Product or GBP**.

Therefore, $GBP = Gain \times Bandwidth$ or $A \times BW$.

Open-loop Frequency Response Curve



For example, from the graph above the gain of the amplifier at 100kHz = 20dB or 10, then the $GBP = 100,000\text{Hz} \times 10 = 1,000,000$.

Similarly, a gain at 1kHz = 60dB or 1000, therefore the $GBP = 1,000 \times 1,000 = 1,000,000$. **The same!**

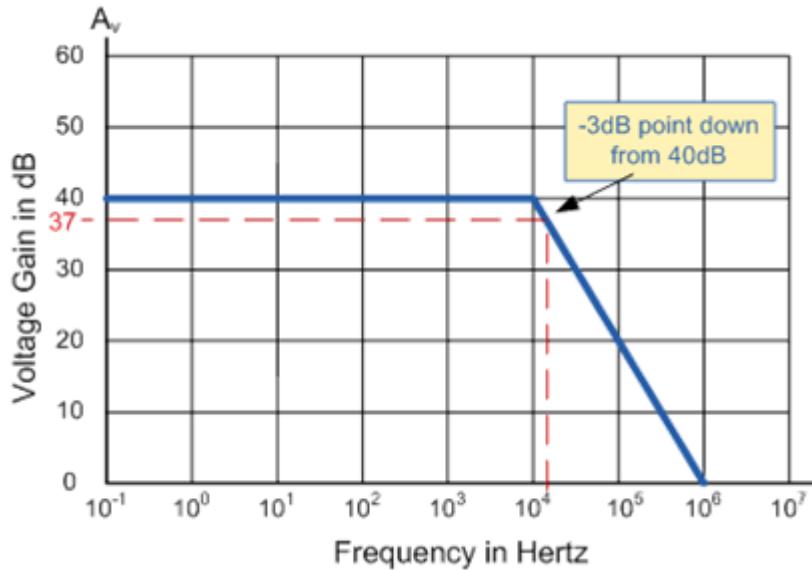
The **Voltage Gain (A)** of the amplifier can be found using the following formula:

$$Gain, A = \frac{V_o}{V_i}$$

and in **Decibels** or (dB) is given as:

$$20 \log A = 20 \log \frac{V_o}{V_i}$$

Bandwidth of Operational Amplifier



The operational amplifiers bandwidth is the frequency range over which the voltage gain of the amplifier is above **70.7%** or **-3dB** (where 0dB is the maximum) of its maximum output value as shown below.

Here we have used the 40dB line as an example. The -3dB or 70.7% of V_{max} down point from the frequency response curve is given as 37dB. Taking a line across until it intersects with the main GBP curve gives us a frequency point just above the 10kHz line at about 12 to 15kHz. We can now calculate this more accurately as we already know the GBP of the amplifier, in this particular case 1MHz.

Example No1.

Using the formula $20 \log (A)$, we can calculate the bandwidth of the amplifier as:

$$37 = 20 \log A \text{ therefore, } A = \text{anti-log} (37 \div 20) = 70.8$$

$$\text{GBP} \div A = \text{Bandwidth, therefore, } 1,000,000 \div 70.8 = 14.124\text{Hz, or } 14\text{kHz}$$

Then the bandwidth of the amplifier at a gain of 40dB is given as **14kHz** as predicted from the graph.

Example No2.

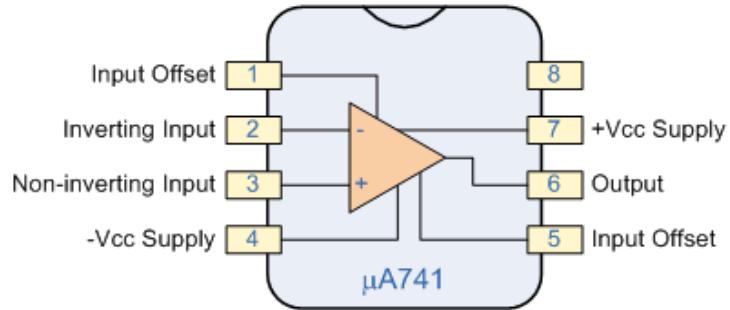
If the gain of the operational amplifier was reduced by half to say **20dB** in the above frequency response curve, the -3dB point would now be at 17dB. This would then give us an overall gain of 7.08, therefore **A = 7.08**. If we use the same formula as above this new gain would give us a bandwidth of **141.2kHz**, ten times more than at 40dB.

It can therefore be seen that by reducing the overall open loop gain of an operational amplifier its bandwidth is increased and vice versa. The -3dB point is also known as the "half power point", as the output power of the amplifier is at half its maximum value at this point.

Op-amp types

Operational amplifiers can be connected using external resistors or capacitors in a number of different ways to form basic "Building Block" circuits such as, Inverting, Non-Inverting, Voltage Follower, Summing, Differential, Integrator and Differentiator type amplifiers. There are a very large number of operational amplifier IC's available to suit every possible application.

The most commonly available and used of all operational amplifiers is the industry standard **741** type IC.



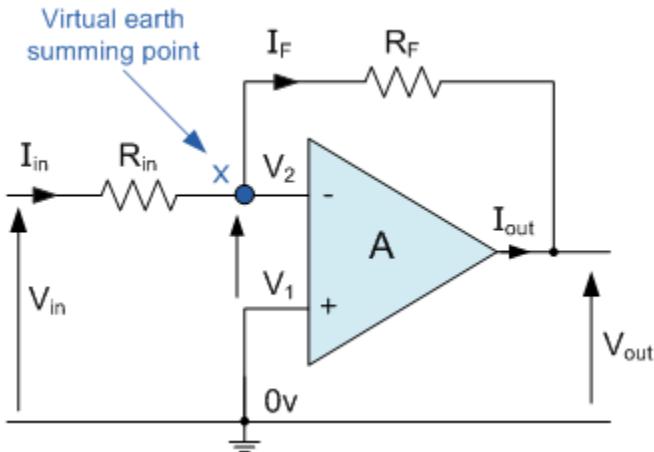
Inverting Amplifier

The open loop gain of an ideal Operational Amplifier can be very high, up to about 1,000,000 (120dB) or more. However, this very high gain is of no real use to us as it makes the amplifier both unstable and hard to control as the smallest of input signals, just a few microvolts, would be enough to cause the output to saturate and swing towards one or the other of the voltage supply rails losing control. As the open loop DC gain of an operational amplifier is extremely high we can afford to lose some of this gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces an effect known commonly as **Negative Feedback**, and thus produces a very stable Operational Amplifier system.

Negative Feedback is the process of "feeding back" some of the output signal back to the input, but to make the feedback negative we must feed it back to the "Negative input" terminal using an external **Feedback Resistor** called R_f . This feedback connection between the output and the inverting input terminal produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its **Closed-loop Gain**.

This results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage giving it the label or term of a *Summing Point*. We must therefore separate the real input signal from the inverting input by using an **Input Resistor**, R_{in} . As we are not using the positive non-inverting input this is connected to a common ground or zero voltage terminal as shown below. But the effect of this closed loop feedback circuit results in the voltage at the inverting input equal to that at the non-inverting input producing a *Virtual Earth* summing point because it will be at the same potential as the grounded reference input.

Inverting Amplifier Circuit



In inverting amplifier circuit the operational amplifier is connected with feedback to produce a closed loop operation. There are two very important rules to remember about inverting amplifiers: "no current flows into the input terminal" and that "V₁ equals V₂". This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a **"Virtual Earth"**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, R_{in}. Then by using these two rules one can find the equation for calculating the gain of an inverting amplifier, using first principles.

Current (i) flows through the resistor network as shown.

$$i = \frac{V_{in}}{R_{in}} = -\frac{V_o}{R_f}$$

The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180° out of phase. This is due to the feedback being negative in value.

Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as.

$$Gain = \frac{V_o}{V_{in}} = -\frac{R_f}{R_{in}}$$

Example No1

Find the closed loop gain of the given inverting amplifier circuit.

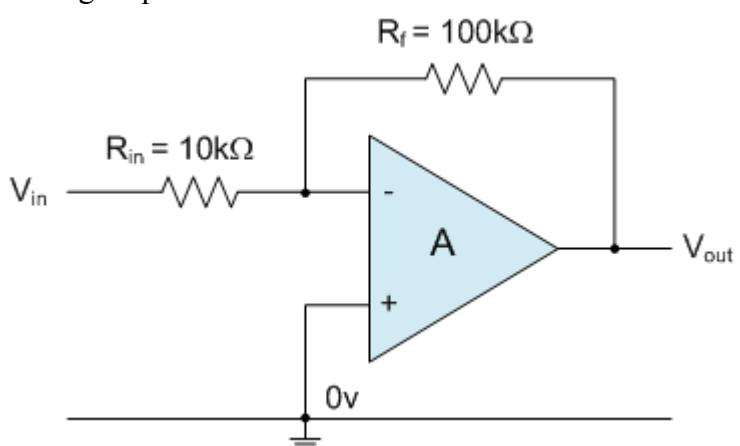
Using the previously found formula for the gain of the circuit

$$Gain = \frac{V_o}{V_{in}} = -\frac{R_f}{R_{in}}$$

R_{in} = 10kΩ and R_f = 100kΩ.

$$Gain = -R_f/R_{in} = 100k/10k = 10.$$

Therefore, the closed loop gain of the given inverting amplifier circuit is given **10** or **20dB**.



Example No2.

The gain of the original circuit is to be increased to **40**, find the new values of the resistors required.

Assume that the input resistor is to remain at the same value of $10\text{ k}\Omega$, then by re-arranging the closed loop voltage gain formula we can find the new value required for the feedback resistor R_f .

$$\text{Gain} = -R_f/R_{in}$$

$$\text{So, } R_f = \text{Gain} \times R_{in}$$

$$R_f = 400,000 \text{ or } 400\text{ k}\Omega$$

The new values of resistors required for the circuit to have a gain of **40** would be,

$$R_{in} = 10\text{ k}\Omega \text{ and } R_f = 400\text{ k}\Omega$$

The formula could also be rearranged to give a new value of R_{in} , keeping the same value of R_f .

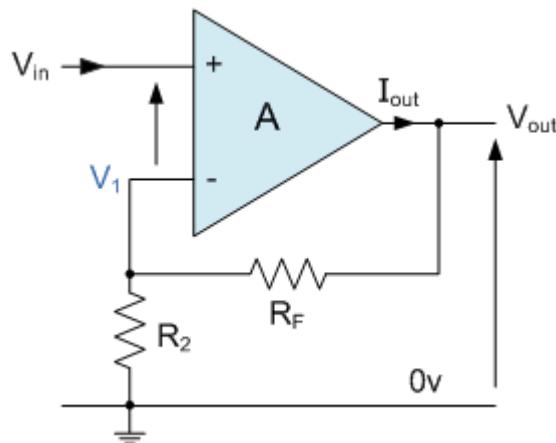
Unity Gain Inverter

One final point to note about **Inverting Amplifiers**, if the two resistors are of equal value, $R_{in} = R_f$ then the gain of the amplifier will be **-1** producing a complementary form of the input voltage at its output as $V_{out} = -V_{in}$. This type of inverting amplifier configuration is generally called a **Unity Gain Inverter** or simply an *Inverting Buffer*.

Non-inverting Amplifier

The second basic configuration of an operational amplifier circuit is that of a **Non-inverting Amplifier**. In this configuration, the input voltage signal, (V_{in}) is applied directly to the Non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit whose output gain is negative in value. Feedback control of the non-inverting amplifier is achieved by applying a small part of the output voltage signal back to the inverting (-) input terminal via a $R_f - R_2$ voltage divider network, again producing negative feedback. This produces a Non-inverting Amplifier circuit with very good stability, a very high input impedance, R_{in} approaching infinity (as no current flows into the positive input terminal) and a low output impedance, r_{out} as shown below.

Non-inverting Amplifier Circuit



Since no current flows into the input of the amplifier, $V_1 = V_{in}$. In other words the junction is a "**Virtual Earth**" summing point. Because of this virtual earth node, the resistors R_f

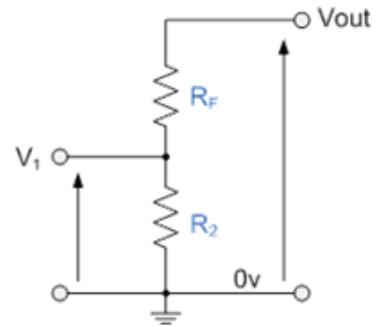
and R_2 form a simple voltage divider network across the amplifier and the voltage gain of the circuit is determined by the ratios of R_2 and R_f as shown below.

Equivalent Voltage Divider Network

Then using the formula to calculate the output voltage of a potential divider network, we can calculate the output Voltage Gain of the **Non-inverting Amplifier** as:

$$V_o = V_{in} \left(1 + \frac{R_f}{R_2}\right)$$

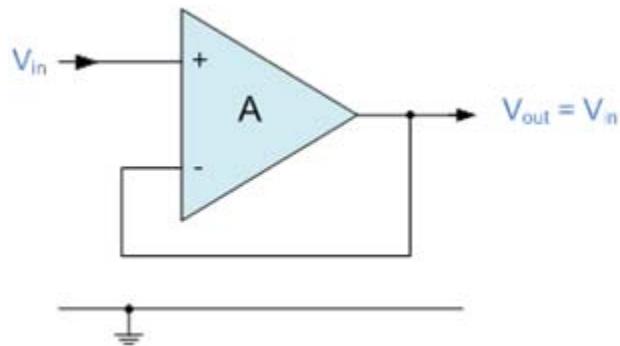
$$Gain = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_2}$$



We can see that the overall gain of a Non-Inverting Amplifier is greater but never less than 1, is positive and is determined by the ratio of the values of R_f and R_2 . If the feedback resistor R_f is zero the gain will be equal to 1, and if resistor R_2 is zero the gain will approach infinity, but in practice it will be limited to the operational amplifiers open-loop differential gain, (A_o).

Voltage Follower (Unity Gain Buffer)

If we made the feedback resistor, $R_f = 0$ then the circuit will have a fixed gain of "1" and would be classed as a **Voltage Follower**. As the input signal is connected directly to the non-inverting input of the amplifier the output signal is not inverted resulting in the output voltage being equal to the input voltage, $V_{out} = V_{in}$. This then makes the Voltage Follower circuit ideal as a *Unity Gain Buffer* circuit because of its isolation properties as impedance or circuit isolation is more important than amplification. The input impedance of the voltage follower circuit is very high, typically above $1M\Omega$.



In this circuit, R_{in} has increased to infinity and R_f reduced to zero, the feedback is 100% and V_{out} is exactly equal to V_{in} giving it a fixed gain of 1 or unity. As the input voltage V_{in} is applied to the non-inverting input the gain of the amplifier is given as:

$$V_o = A(V_{in} - V_o)$$

$$V_{in} = V_+ \quad V_o = V_-$$

$$Gain = \frac{V_o}{V_{in}} = 1$$

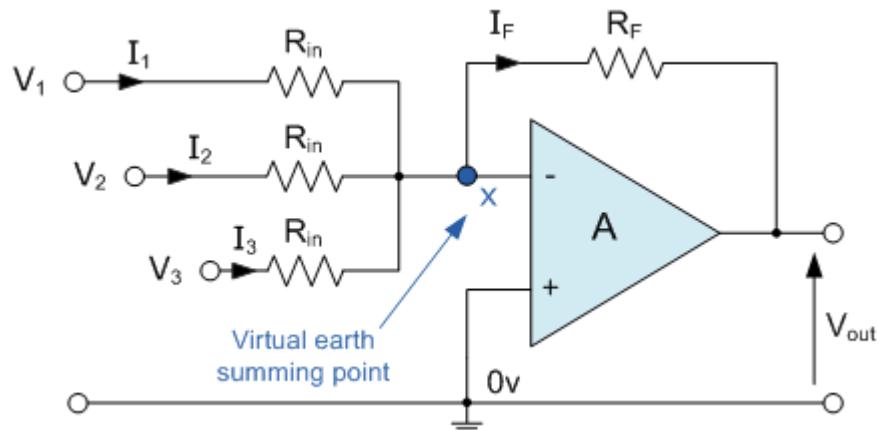
The voltage follower or unity gain buffer is a special and very useful type of **Non-inverting amplifier** circuit that is commonly used in electronics to isolate circuits from each other especially in High-order state variable or Sallen-Key type active filters to separate one filter stage from the other. Typical digital buffer IC's available are the 74LS125 Quad 3-state buffer or the more common 74LS244 Octal buffer.

One final thought, the output voltage gain of the voltage follower circuit with closed loop gain is **Unity**, the voltage gain of an ideal operational amplifier with open loop gain (no feedback) is infinite. Then by carefully selecting the feedback components we can control the amount of gain produced by an Operational Amplifier anywhere from 1 to infinity.

Summing Amplifier

The **Summing Amplifier** is a very flexible circuit based upon the standard *Inverting Operational Amplifier* configuration. We saw previously that the inverting amplifier has a single input signal applied to the inverting input terminal. If we add another input resistor equal in value to the original input resistor, R_{in} we end up with another operational amplifier circuit called a **Summing Amplifier**, "Summing Inverter" or even a "Voltage Adder" circuit as shown below

Summing Amplifier Circuit



The output voltage, (V_{out}) now becomes proportional to the sum of the input voltages, V_1 , V_2 , V_3 etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = - \left[\frac{V_1}{R_{in}} + \frac{V_2}{R_{in}} + \frac{V_3}{R_{in}} \right]$$

$$\text{then, } V_{out} = - \frac{R_F}{R_{in}} (V_1 + V_2 + V_3)$$

The **Summing Amplifier** is a very flexible circuit indeed, enabling us to effectively "Add" or "Sum" together several individual input signals. If the input resistors are all equal a unity gain inverting adder can be made. However, if the input resistors are of different values a "scaling summing amplifier" is produced which gives a weighted sum of the input signals.

Example No1

Find the output voltage of the following *Summing Amplifier* circuit.

The gain of the circuit

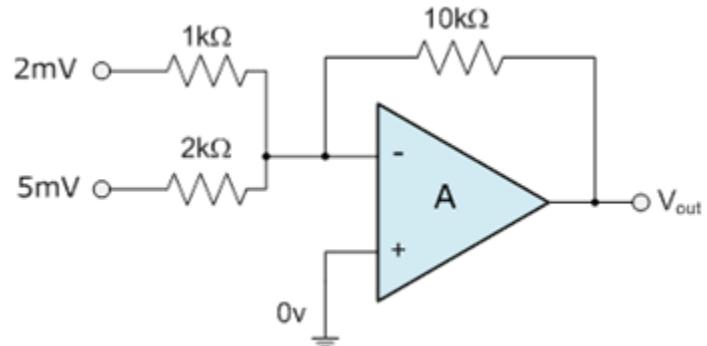
$$Gain = \frac{V_o}{V_{in}} = -\frac{R_f}{R_{in}}$$

substituting the values of the resistors,

$$A_1 = \frac{10k\Omega}{1k\Omega} = -10, \quad A_2 = \frac{10k\Omega}{2k\Omega} = -5$$

The output voltage is the sum of the two amplified input signals:

$$V_o = (-10(2mV)) + (-5(5mV)) \\ = -45mV$$

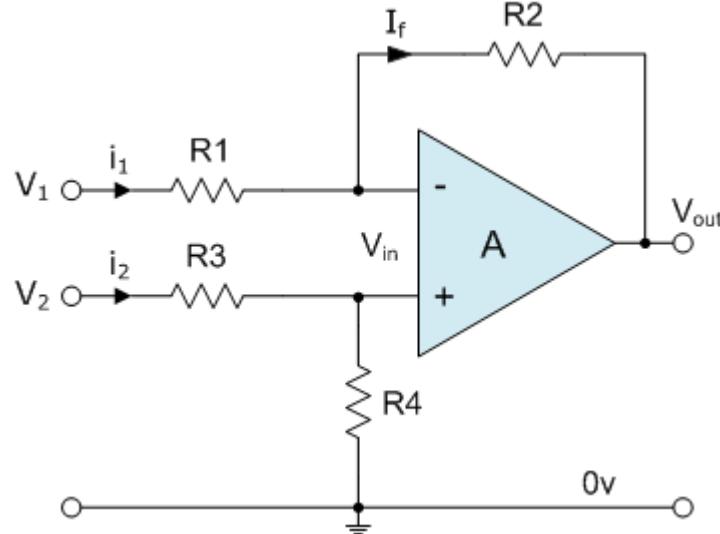


If the input resistances of a summing amplifier are connected to potentiometers the individual input signals can be mixed together by varying amounts. For example, for measuring temperature, you could add a negative offset voltage to make the display read "0" at the freezing point or produce an audio mixer for adding or mixing together individual waveforms (sounds) from different source channels (vocals, instruments, etc) before sending them combined to an audio amplifier.

Differential Amplifier

Up to now we have used only one input to connect to the amplifier, using either the "Inverting" or the "Non-inverting" input terminal to amplify a single input signal with the other input being connected to ground. But we can also connect signals to both of the inputs at the same time producing another common type of operational amplifier circuit called a differential amplifier. The resultant output voltage will be proportional to the "Difference" between the two input signals, V_1 and V_2 . This type of circuit can also be used as a subtractor.

Differential Amplifier Circuit



The transfer function for a differential amplifier circuit is given as:

$$V_o = -\frac{R_2}{R_1}V_1 + (1 + \frac{R_2}{R_1})(\frac{R_4}{R_3 + R_4})V_2$$

When $R_1 = R_3$ and $R_2 = R_4$ the transfer function formula can be modified to the following:

$$V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

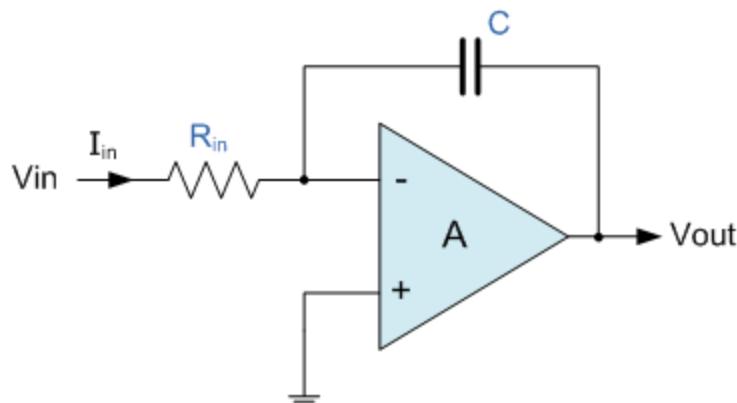
If all the resistors are all of the same ohmic value the circuit will become a **Unity Gain Differential Amplifier** and the gain of the amplifier will be 1 or Unity.

One major limitation of this type of amplifier design is that its input impedances are lower compared to that of other operational amplifier configurations, for example, a non-inverting (single-ended input) amplifier. Each input voltage source has to drive current through an input resistance, which has less overall impedance than that of the op-amps input alone. One way to overcome this problem is to add a *Unity Gain Buffer Amplifier* such as the voltage follower seen in the previous tutorial to each input resistor. This then gives us a differential amplifier circuit with very high input impedance and is the basis for most "Instrumentation Amplifiers", mainly used to amplify very small differential signals from strain gauges, thermocouples or current sensing resistors in motor control systems.

The Integrator Amplifier

Till now we saw how an operational amplifier can be used as part of a positive or negative feedback amplifier or as an adder or subtractor type circuit using pure resistors in both the input and the feedback loop. But what if we were to change the purely Resistive (R_f) feedback element of an inverting amplifier to that of a reactive element, such as a *Capacitor*, C . We now have a resistor and capacitor combination forming an *RC Network* across the operational amplifier as shown below.

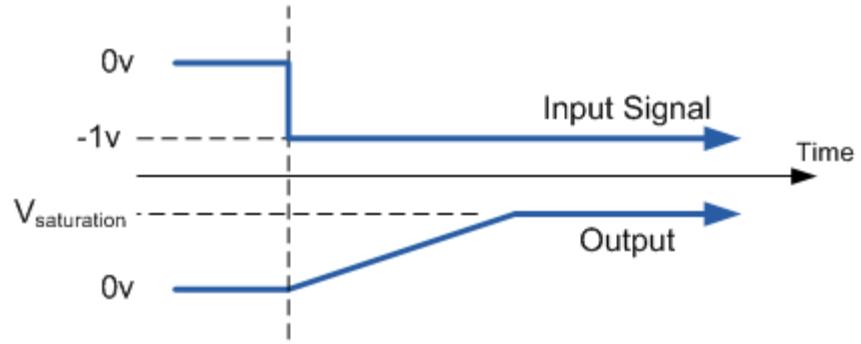
Integrator Amplifier Circuit



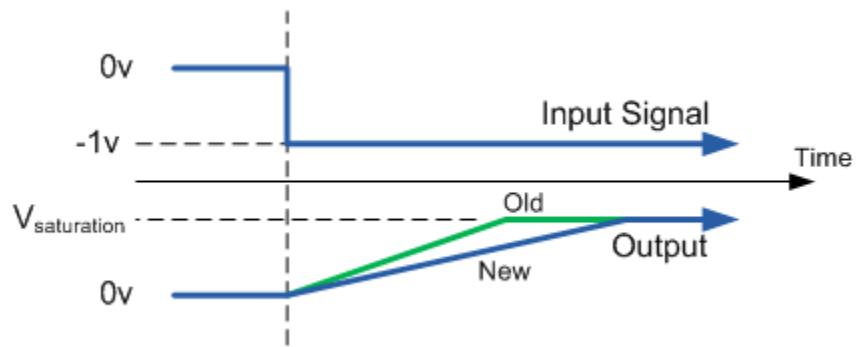
The integrator amplifier performs the mathematical operation of **integration**, that is, we can cause the output to respond to changes in the input voltage over time and the integrator amplifier produces a voltage output which is proportional to that of its input voltage with respect to time. In other words the magnitude of the output signal is determined by the length of time a

voltage is present at its input as the current through the feedback loop charges or discharges the capacitor.

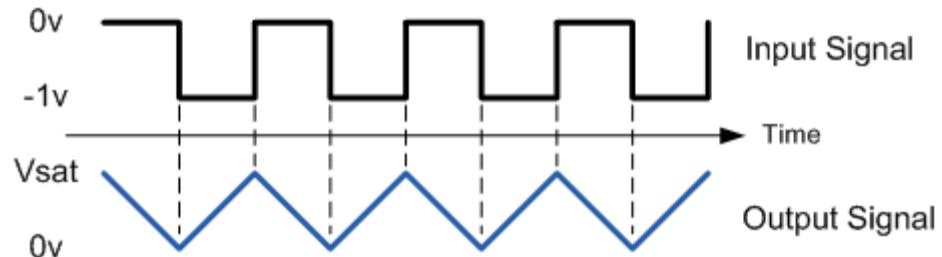
When a voltage, V_{in} is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit (voltage follower circuit) giving an overall gain of less than 1, thus resulting in zero output. As the feedback capacitor C begins to charge up, the ratio of Z_f/R_{in} increases producing an output voltage that continues to increase until the capacitor is fully charged. At this point the ratio of feedback capacitor to input resistor (Z_f/R_{in}) is infinite resulting in infinite gain and the output of the amplifier goes into saturation as shown in the diagram. (Saturation is when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with no control in between).



The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, "RC time constant". By changing this RC time constant value, either by changing the value of the Capacitor, C or the Resistor, R , the time in which it takes the output voltage to reach saturation can also be changed.



If we apply a constantly changing input signal such as a square wave to the input of an **Integrator Amplifier** then the capacitor will charge and discharge in response to changes in the input signal. This results in an output signal with a sawtooth waveform and its frequency is dependent upon the time constant (RC) of the circuit. This type of circuit is also known as a **Ramp Generator** and the transfer function is given below.



Since the node voltage of the integrating op-amp at its inverting input terminal is zero, the current I_{in} flowing through the input resistor is given as:

$$I_{in} = \frac{V_{in}}{R}$$

The current flowing through the feedback capacitor C is given as:

$$I_{in} = C \frac{dV_{out}}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$\frac{V_{in}}{R} = C \frac{dV_{out}}{dt} = 0$$

From which we have an ideal voltage output for the Integrator Amplifier as:

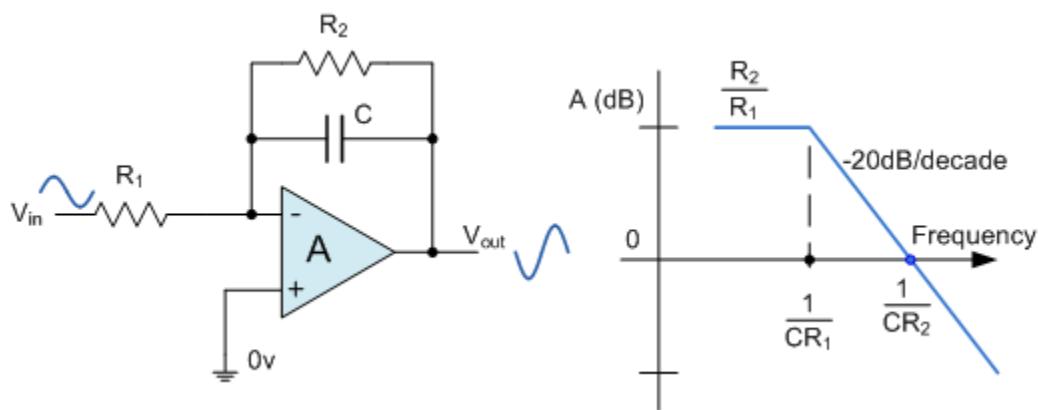
$$V_{out} = -\frac{1}{RC} \int V_{in} dt = -\frac{1}{j\omega RC} V_{in}$$

Where $j\omega = 2\pi f$ and the output voltage V_{out} is a constant $1/RC$ times the integral of the input voltage V_{in} with respect to time. The minus sign (-) indicates a 180° phase shift because the input signal is connected directly to the inverting input terminal of the op-amp.

Active Low Pass Filter

If we changed the above square wave input signal to that of a sine wave of varying frequency the **Integrator Amplifier** begins to behave like an active "Low Pass Filter", passing low frequency signals while attenuating the high frequencies. However, at DC (0Hz) the capacitor acts like an open circuit blocking any feedback voltage resulting in zero negative feedback from the output back to the input of the amplifier. Then the amplifier effectively is connected as a normal open-loop amplifier with very high open-loop gain resulting in the output voltage saturating.

The addition of a large value resistor, R_2 across the capacitor, C gives the circuit the characteristics of an inverting amplifier with finite closed-loop gain of R_2/R_{in} at very low frequencies while acting as an integrator at higher frequencies. This then forms the basis of an *Active Low Pass Filter*.



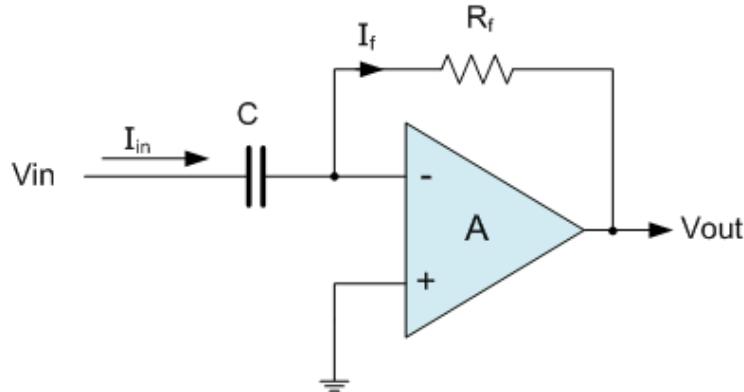
The AC Integrator with DC Gain Control

The Differentiator Amplifier

The basic differentiator amplifier circuit is the exact opposite to that of the *Integrator* operational amplifier circuit. Here, the position of the capacitor and resistor have been reversed and now the Capacitor, C is connected to the input terminal of the inverting amplifier while the Resistor, R_f forms the negative feedback element across the operational amplifier. This circuit performs the mathematical operation of **Differentiation**, i.e. it produces a voltage output which is proportional to **rate-of-change** of the input voltage and the current flowing through the capacitor. In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response becoming more of a "spike" in shape.

As with the integrator circuit, we have a resistor and capacitor forming an RC Network across the operational amplifier and the reactance (X_c) of the capacitor plays a major role in the performance of a differentiator amplifier.

Differentiator Amplifier Circuit



Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$i_{IN} = I_F \quad \text{and} \quad I_F = -\frac{V_o}{R_F}$$

The Charge on the Capacitor = Capacitance x Voltage across the Capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C \frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current i

$$i_{IN} = C \frac{dV_{IN}}{dt} = I_F$$

From which we have an ideal voltage output for the Differentiator Amplifier is given as:

$$V_o = -R_f C \frac{dV_{in}}{dt}$$

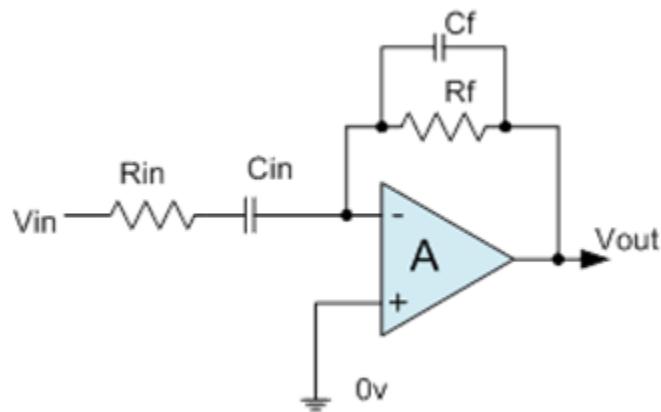
Therefore, the output voltage V_{out} is a constant $-R_f C$ times the derivative of the input voltage V_{in} with respect to time. The minus sign indicates a 180° phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

Active High Pass Filter

The capacitor blocks any DC content only allowing AC type signals whose frequency is dependent on the rate of change of the input signal, to pass through. At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R_f/X_c) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier. Thus with sinusoidal wave at the input this circuit will act as an active high pass filter circuit.

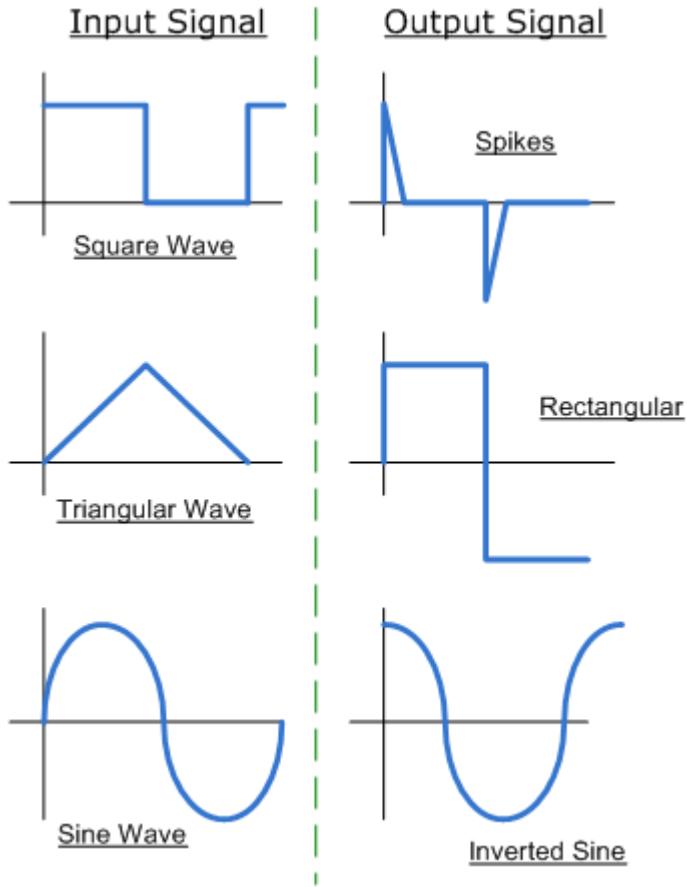
The basic single resistor and single capacitor differentiator circuit is not widely used to reform the mathematical function of differentiation because of the two inherent faults mentioned above: Instability and Noise.

At high frequencies a differentiator circuit becomes unstable and will start to oscillate. To avoid this, the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor, C_f , across the feedback resistor R_f . Also, the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage. So some means of limiting the bandwidth in order to achieve closed-loop stability is required. In order to reduce the overall closed-loop gain of the circuit at high frequencies, an extra Resistor, R_{in} is added to the input as shown below. Thus, the new circuit acts like a Differentiator amplifier at low frequencies and an amplifier with resistive feedback at high frequencies giving much better noise rejection.



Differentiator Waveforms

If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependent upon the RC time constant of the Resistor/Capacitor combination.



Lab# 1(A): Study of Basic OPAMP Configurations and Simple Mathematical Operations

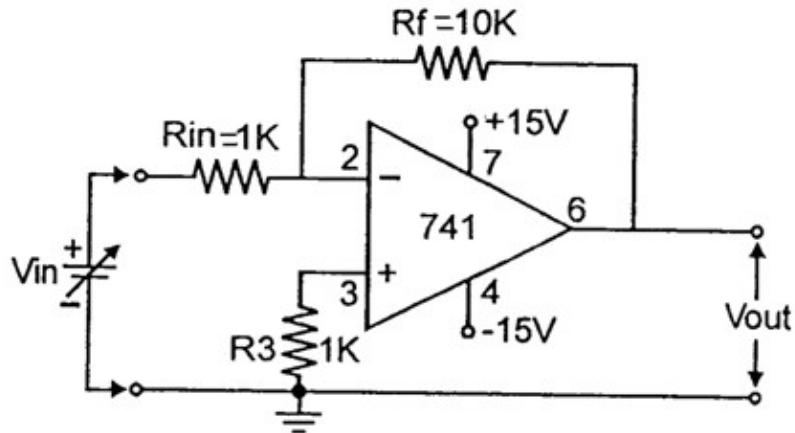
Objectives:

- (I) Study of the inverting amplifier configuration and to find its gain
- (II) Study of the non-inverting amplifier configuration and to find its gain
- (III) Study simple mathematical operation and design an averaging amplifier

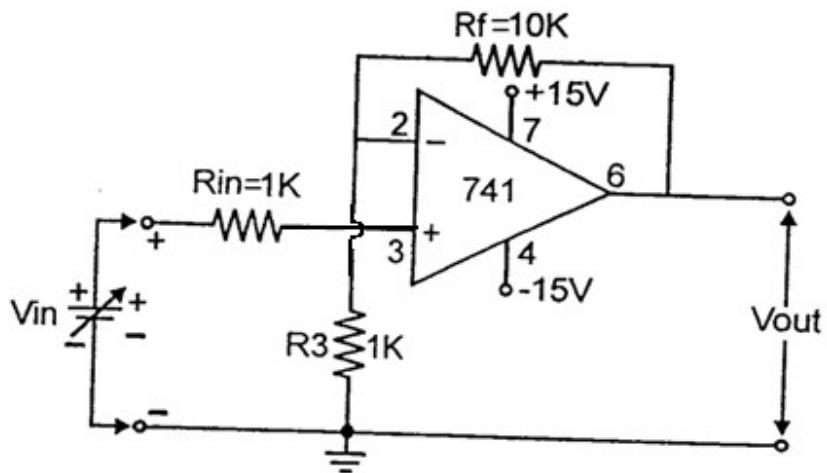
Components: OPAMP 741 chip, Resistors, Oscilloscope, DC voltage source, Bread board

Theory: Please refer the supplementary note.

Circuit Diagram:



Inverting amplifier



Non-inverting amplifier

Procedure:

(I) Inverting amplifier

1. Configure the circuit as shown in the circuit diagram. Connect the pins 7 and 4 of the IC to the $\pm 15V$ output terminals of the D.C. power supply. Connect the 0V terminal to ground. Choose $R_{in} = 1K\Omega$ and $R_f = 10K\Omega$. Measure the resistance values with multimeter and calculate gain, $-(R_f/R_{in})$. Connect a resistor $R_3 (= R_{in} \parallel R_f \approx R_{in})$ as shown in the circuit diagram so as to minimize offset due to input bias current.
2. Connect one of the output terminals of the D.C. power supply (0-30V) at the **inverting input (pin no. 2)**.
3. Switch on the power supply and apply different voltages in the range 0- 1.5V (why?) in steps of 0.2 V at the inverting terminal. Measure this input using a digital multimeter.
4. Measure the corresponding output voltages with the multimeter and calculate gain V_o/V_{in} . Note the sign of the output voltage.
5. Now, replace R_f by $50K\Omega$. Measure the resistance value with multimeter and calculate gain, $-(R_f/R_{in})$.
6. Apply different voltages in the range 0- 0.5V in steps of 0.1 V at the inverting terminal. Measure this input using a digital multimeter.
7. Measure the corresponding output voltages with the multimeter and calculate gain V_o/V_{in} .
8. Plot graphs for $V_{in} \sim V_o$ for both the values of R_f .
9. You may also use a function generator to give a sinusoidal input and notice the output waveform using an oscilloscope.

(II) Non-inverting amplifier

1. Configure the circuit as shown in the circuit diagram with $R_{in} = 1K\Omega$ and $R_f = 10K\Omega$. using the measured value of resistance calculate gain, $1 + (R_f/R_{in})$.
2. Connect one of the output terminals of the D.C. power supply (0-30V) at the **non-inverting input (pin no. 3)**.
3. Repeat steps 3 onwards of procedure (I) with inputs applied at non-inverting terminal.

Observations

Table (I):

| Obs. No. | Input (V) | $-\frac{R_f}{R_{in}} = \text{-----}$ | | | $-\frac{R_f}{R_{in}} = \text{-----}$ | | |
|----------|-----------|--------------------------------------|-------------------|---------|--------------------------------------|-------------------|---------|
| | | Output (V) | Gain V_o/V_{in} | Average | Output (V) | Gain V_o/V_{in} | Average |
| | 0.2 | | | | | | |
| | 0.4 | | | | | | |
| | ... | | | | | | |

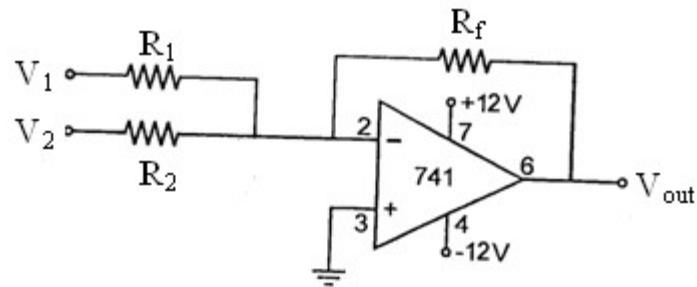
Table (For II):

| Obs. No. | Input (V) | $1 + \frac{R_f}{R_{in}} = \text{-----}$ | | | $1 + \frac{R_f}{R_{in}} = \text{-----}$ | | |
|----------|-----------|---|-------------------|---------|---|-------------------|---------|
| | | Output (V) | Gain V_o/V_{in} | Average | Output (V) | Gain V_o/V_{in} | Average |
| 1 | 0.1 | | | | | | |
| 2 | 0.2 | | | | | | |
| .. | ... | | | | | | |

(III) Simple mathematical operations using OPAMP

a. To study OPAMP as summing amplifier

Circuit Diagram:



Procedure:

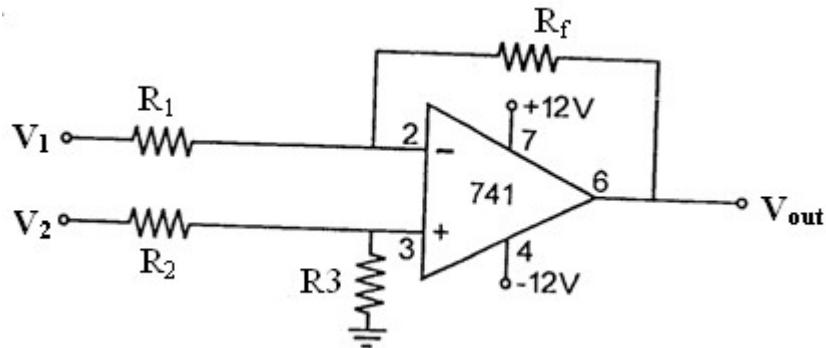
1. Assemble the circuit as shown in circuit diagram choosing $R_1, R_2, R_f = 10K\Omega$ each. Use $0- \pm 15V$ terminal output to provide supply to the IC.
2. Using $0 - 30V$ and $5V$ terminals of the power supply, apply two inputs at the inverting terminal. Measure each input with multimeter.
3. Measure the output with multimeter for at least five input combinations.
4. Compare the output with the sum of the two inputs.

Observations:

| Obs.No | V_1 (V) | V_2 (V) | V_{out} (V) | $V_1 + V_2$ (V) |
|--------|-----------|-----------|---------------|-----------------|
| 1 | | | | |
| .. | | | | |
| 5 | | | | |

b. To study OPAMP as difference amplifier

Circuit Diagram:



Procedure:

1. Assemble the circuit as shown in circuit diagram choosing $R_1, R_2, R_3, R_f = 10K\Omega$ each. Use $0- \pm 15V$ terminal output to provide supply to the IC.
2. Using $0 - 30V$ and $5V$ terminals of the power supply, apply two inputs, one at the inverting and the other at the non-inverting terminal. Measure each input with multimeter.
3. Measure output with multimeter for at least five input combinations.
4. Compare the output with the difference of the two inputs.

Observations:

| Obs.No | V_1 (V) | V_2 (V) | V_{out} (V) | $V_2 - V_1$ (V) |
|--------|--------------|--------------|------------------|--------------------|
| 1 | | | | |
| .. | | | | |
| 5 | | | | |

c. Inverting amplifier configuration of OPAMP is nothing but multiplication or division of input voltage with a number equal to R_f/R_1 . With the knowledge of division and addition design an averaging amplifier of inputs V_1 and V_2 and tabulate.

Conclusions:

Lab#1(B): Applications of OPAMP as Comparator and Schmitt Trigger

Objectives:

- (i) Study of OPAMP as comparator
- (ii) Study of OPAMP as Schmitt trigger

(i) Comparator

Theory

When the feedback signal (voltage) is applied to the inverting (-) input of the op-amp then the feedback is negative. Negative feedback tends to reduce the difference between the voltages at the inverting and non-inverting terminals and make linear circuits. Without negative feedback the op-amp output is highly sensitive to the input, which can be used to design *switching* or *nonlinear* circuits. The voltage *comparator* is a device which uses no feedback; then saturation is the desired result. In this circuit we want a simple yes-no answer to be signified by either positive saturation or negative saturation of the output.

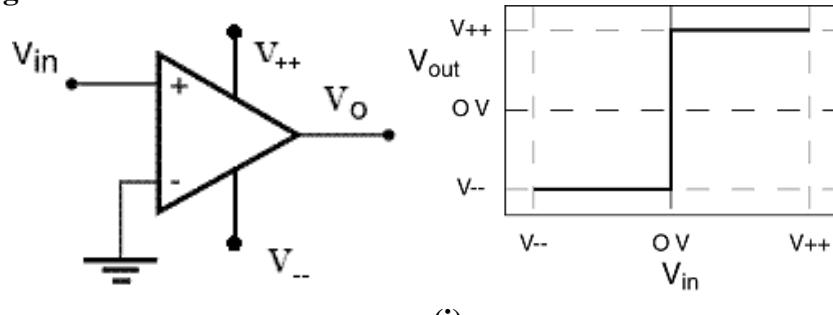
In the circuit diagrams shown below, for Fig.(i), if $V_{in} > 0$, $V_o \approx V_{++}$ and if $V_{in} < 0$, $V_o \approx V_{--}$. The output is no longer linearly related to the input— it's more like a digital signal, high or low depending on how V_{in} compares to ground (0 V). Needless to mention that, if V_{in} is applied at the inverting terminal with respect to a grounded non-inverting terminal, the output will switch to low when $V_{in} > 0$. Figure (ii) shows a small modification, allowing the circuit to switch its output when V_{in} crosses a certain preset voltage level, often called the **threshold voltage**, V_{th} .

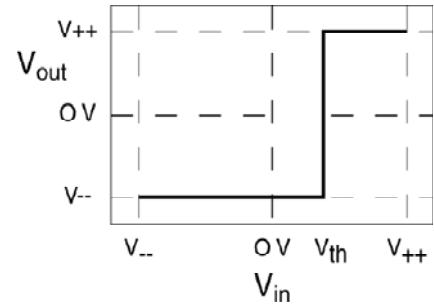
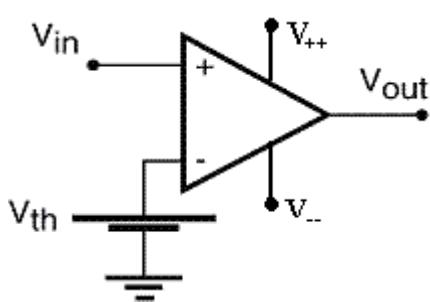
Typical applications of this circuit are crossover detectors, analog to digital converters or counting applications where one wants to count pulses that exceed a certain voltage level.

Components/Equipments:

- (i) OPAMP (IC-741) chip, (ii) A D.C. power supply, (iii) A digital multimeter (DMM), (iv) A digital storage oscilloscope (DSO), (v) Connecting wires, (vi) Breadboard

Circuit Diagram:





(ii)

Procedure:

1. Construct the comparator circuit on the breadboard as shown in the circuit diagram. Take care to give proper connections at the desired pins of the IC.
2. Use terminal **C** of the d.c. power supply (denoted by V_+ and V_- knobs) to provide power supply to IC. Connect the $0V$ terminal to ground.
3. Connect terminal **A** of the d.c. power supply (0-30V) at the input. Use terminal **B** (5V) to provide threshold voltage V_{th} for circuit shown in Fig. (ii).
4. Vary the input from a negative value to a positive value through 0.
5. Using the DMM, measure and tabulate V_{in} and V_{out} . You can also look at the output using a DSO by coupling the output to it in DC mode.
6. Make a plot of V_{out} vs V_{in} for each circuit. Estimate V_{th} from graph for Fig. (ii) and compare with the V_{th} value actually applied. You can repeat the same procedure for different values of threshold.
7. Repeat the entire procedure described above with input at the inverting terminal and the non-inverting terminal being grounded w/o and with the threshold voltage connected to it.

Observations:

For Fig. (i)

| Obs.No | V_i (V) | V_o (V) |
|--------|--------------|--------------|
| 1 | | |
| .. | | |
| .. | | |

For Fig. (ii)

| Obs.No | V_i (V) | V_o (V) |
|--------|--------------|--------------|
| 1 | | |
| .. | | |
| .. | | |

Disscusions:

Discuss the graphs you obtained.

Precautions:

(ii) Schmitt trigger

The Schmitt trigger is a variation of the simple comparator which has hysteresis, that is, it has a toggle action. It uses a positive feedback. When the output is high, positive feedback makes the switching level higher than it is when the output is low. A little positive feedback makes a comparator with better noise immunity.

Now, to understand what causes the hysteresis let's analyze the circuit diagram given below, using the same rules as in the previous section for the comparator. The key in understanding this circuit will again be in calculating the voltages that cause its output to switch. If V_+ and V_- are the actual voltages at the non-inverting and inverting terminals of the OPAMP, then the output will be the following, considering that $V_- = 0$:

$$\begin{aligned} \text{if } V_+ > 0, \quad & V_{\text{out}} \approx V_{++} \\ \& \text{if } V_+ < 0, \quad V_{\text{out}} \approx V_{--} \end{aligned}$$

Since V_{out} changes its state whenever V_+ crosses 0V, we need to find what value of V_{in} results in $V_+ = 0$. The two values of V_{in} for which the output switches are called the trip points. V_+ acts as a voltage divider formed by R_1 and R_2 between V_{in} and V_{out} . Thus the trip points of a noninverting Schmitt trigger are:

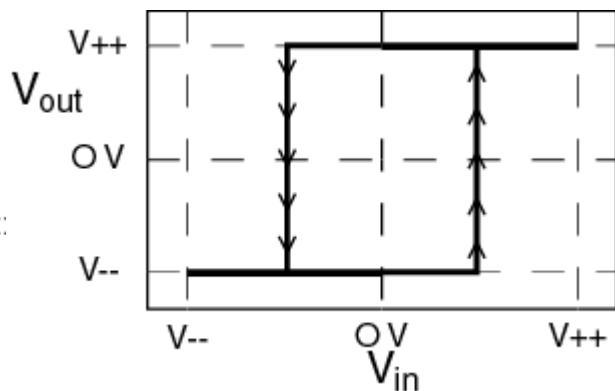
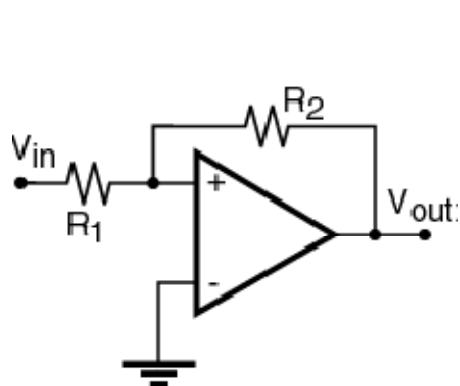
$$\begin{aligned} V_{\text{in}} &= -V_{\text{out}} (R_1/R_2) \text{ (Lower trip point, LTP)} \\ &= +V_{\text{out}} (R_1/R_2) \text{ (Upper trip point, UTP)} \end{aligned}$$

Choosing suitable ratios of R_1 to R_2 , enough hysteresis can be created in order to prevent unwanted noise triggers.

Components/Equipments:

- (i) OPAMP (IC-741) chip
- (ii) A D.C. power supply
- (iii) A digital multimeter
- (iv) Connecting wires
- (v) Breadboard
- (vi) Digital storage oscilloscope (DSO)

Circuit Diagram:



Procedure:

1. Construct the schmitt trigger circuit on the breadboard as shown in the circuit diagram.
2. Connect the d.c. power supply at the input. Vary the input from a negative value through 0.
3. Using the DMM, measure and tabulate V_{in} and V_{out} .
4. Make a plot of V_{out} vs V_{in} . Estimate the trip points from the graph and compare with the computed value, i.e. $V_{in} = \pm V_{out} R_1 / R_2$
5. You can also look at the output using a DSO by coupling the output to it in DC mode.

Observations:

| Obs.No | V_i (V) | V_o (V) |
|--------|-----------|-----------|
| 1 | | |
| .. | | |
| .. | | |

Discussions:

Analyze the graph you obtained. Discuss the switching action.

Precautions:

Lab#2a: Differentiation and Integration using OPAMP

Objectives:

- (I) To study OPAMP as a differentiator
- (II) To study OPAMP as an integrator

Apparatus:

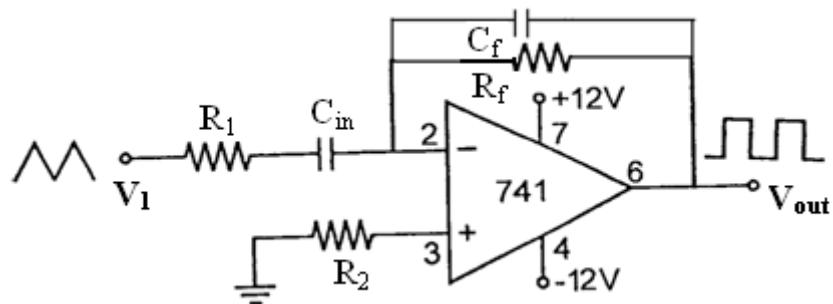
1. OPAMP IC 741
2. D.C. power supply
3. Resistors
4. Digital multimeter
5. Connecting wires
6. Breadboard
7. Function generator
8. Digital storage oscilloscope

Theory:

Please refer to the supplementary note.

(I) To study OPAMP as a differentiator

Circuit Diagram of practical differentiator:



Differentiator action can be performed by the circuit given in supplementary material, which consists of only R_f in the feedback and input capacitor C_{in} with a gain equal to R_f/C_{in} . With increase in frequency gain, R_f/C_{in} increases which makes differentiator unstable. Further input impedance decreases at high frequency, which makes noise to amplify and override the signal. For the practical differentiator, C_f is added in parallel to R_f to control the gain and a small resistance R_1 at the input in series with C_{in} drops the noise at the input. R_2 is known as offset minimizing resistor (R_{OM}) which reduces output offset voltage due to input bias current.

Procedure:

1. Assemble the circuit as shown in circuit diagram choosing $R_1, R_2 = 1\text{K}\Omega$ each, $R_f = 10\text{K}\Omega$, $C_{in} = 0.1 \mu\text{F}$ and $C_f = 0.01\mu\text{F}$. Use 0- $\pm 15\text{V}$ terminal output to provide supply to the IC.
2. Feed a triangular input signal of required amplitude from the function generator, which is set at 1K frequency.
3. Feed both the input and output signals to an oscilloscope and save. The output should be approximately a square wave.
4. Check the output waveform with sine and square waves as inputs and save.

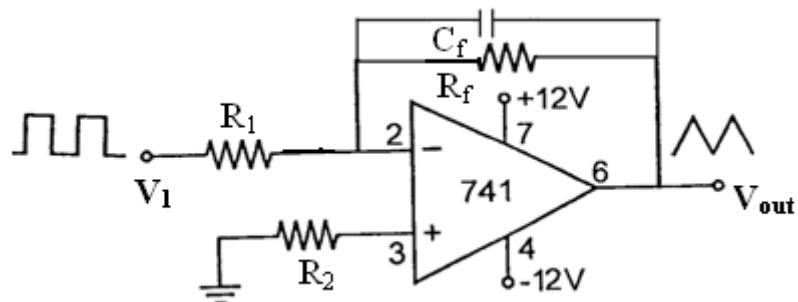
Observations: (Paste the various input and corresponding output waveforms here)

| Observation | Waveform | | |
|-------------|----------|------|--------|
| | Input | sine | square |
| Output | | | |

Discussions

(VII) To study OPAMP as an integrator

Circuit Diagram of practical integrator



In this practical integrator circuit R_f is connected parallel with C_f which is absent in the integrator circuit given in supplementary material. R_f discharges left over charges present in the capacitor before next pulse being applied and limits the gain of the circuit at low frequencies, which is infinite at D.C. R_2 is known as offset minimizing resistor (ROM) which reduces output offset voltage due to input bias current.

Procedure:

2. Assemble the circuit as shown in circuit diagram choosing $R_1, R_2 = 10\text{K}\Omega$ each, $R_f = 100\text{K}\Omega$, and $C_f = 0.1\mu\text{F}$. Use 0- $\pm 15\text{V}$ terminal output to provide supply to the IC. Feed a

square wave input of required amplitude from the function generator, which is set at $1\text{K}\Omega$ frequency.

3. Feed both the input and output signals to an oscilloscope. The output should be a triangular wave.

Observations: (Paste the various input and corresponding output waveforms here)

| Observation | Waveform |
|-------------|----------|
| Input | |
| Output | |

Lab#2b: Active filter using OPAMP

Objective:

- (I) To construct a low pass active filter using OPAMP

Filters: The main disadvantage of passive filters (as you have already seen in one of your previous labs) is the fact that the maximum gain that can be achieved with these filters is 1. In other words, the maximum output voltage is equal to the input voltage. If we make filter circuits using Opamps, then the gain can be greater than 1.

The circuits employed are all based on the inverting Opamps with the addition of a capacitor placed in the correct position for the particular type of filter. These circuits are called active filter circuits because they use Opamps which require a power supply.

Low-Pass filters - the integrator reconsidered

A low pass filter passes only low frequency signals and attenuates signals of high frequencies. We have already considered the time response of the integrator circuit, but its frequency response can also be studied. Figure 1 shows a low pass active filter in inverting configuration.

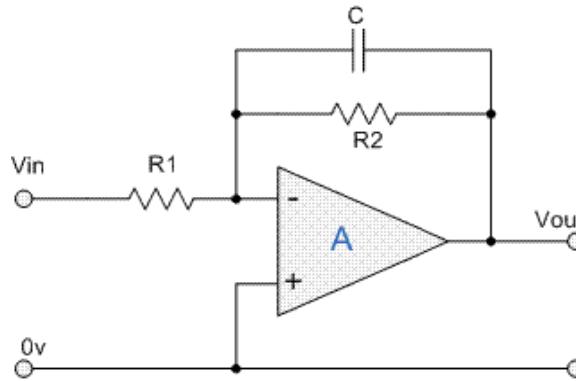


Fig. 1: First Order Low Pass Filter with Op Amp

Gain of the above circuit, $A_v = -\frac{R_2|X_c|}{R_1}$,

where $X_c = \frac{1}{2\pi f C}$, is the impedance of the capacitor and f is the frequency of the input signal.

At high frequencies the capacitor acts as a short, so the gain of the amplifier approaches zero. At very low frequencies the capacitor is open and the gain of the circuit is $-(R_2/R_1)$. We can consider the frequency to be high when the large majority of current goes through the capacitor; i.e., when the magnitude of the capacitor impedance is much less than that of R_2 . In other words, we have high frequency when $X_c \ll R_2$. Since R_2 now has little effect on the circuit, it should act as an integrator. Likewise low frequency occurs when $R_2 \ll X_c$, and the circuit will act as an amplifier with gain $-R_2/R_1$. Thus, the cut-off frequency is given as $f_c = \frac{1}{2\pi R_2 C}$ and the

frequency response is as shown below (Fig.2). The frequency response curve of the filter decreases by 20dB/Decade or 6dB/Octave from the determined cut-off frequency point which is always at -3dB below the maximum gain value.

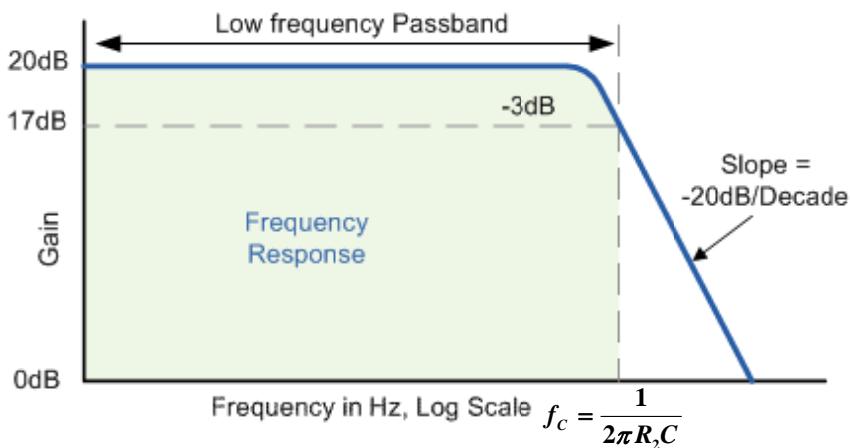


Fig. 2: Frequency response curve of an active low pass filter

Similarly high pass filter can be constructed with differentiator circuit and using a low pass filter and high pass filter, a band pass filter can be constructed.

Procedure:

1. Read/measure the values of all circuit components to be used. Calculate the cut-off frequencies in each case.
2. Using the scope set the function generator to produce an input voltage of approximately 100 mV(pp) sine wave.
3. Set up the low/high/band pass active filter on the breadboard as shown in the circuit diagrams. Connect the function generator to apply input. Use the dual trace oscilloscope to look at both V_{in} and V_{out} . Be sure that the two oscilloscope probes have their grounds connected to the function generator ground. Match the magnification control both at the probe and the oscilloscope.
4. Set the RANGE of the function generator between 20 Hz to 20 kHz. Measure the $V_{in}(pp)$ and $V_{out}(pp)$. Use **digital filter** or **average** options from oscilloscope to measure voltages whenever needed.
5. From your measurements determine the gain, $\frac{V_o(pp)}{V_{in}(pp)}$ and compare with the calculated value.
6. Plot $\log f \sim \text{gain (dB)}$.

Observations:

(I) For Low Pass Filter:

$$R_1 = \text{_____}, \quad R_2 = \text{_____}, \quad C = \text{_____},$$

$$\text{Max Gain(calculated)} = -\frac{R_2}{R_1} = \text{_____}, \quad f_c = \frac{1}{2\pi R_2 C} = \text{_____}$$

Table:

| Sl. No. | Frequency, f (kHz) | $V_{in}(pp)$ (Volt) | $V_o(pp)$ (Volt) | Gain, $A_v = \frac{V_o(pp)}{V_i(pp)}$ | Gain (dB) |
|---------|--------------------|---------------------|------------------|---------------------------------------|-----------|
| 1 | | | | | |
| 2 | | | | | |
| .. | | | | | |
| .. | | | | | |

Lab#3: Phase Shift Oscillator using Opamps

Objectives:

To construct and determine the resonant frequency of

- (i) A phase shift oscillator

Overview:

The main principle of oscillator is positive feedback. Block diagram of oscillator is shown in Figure 1.

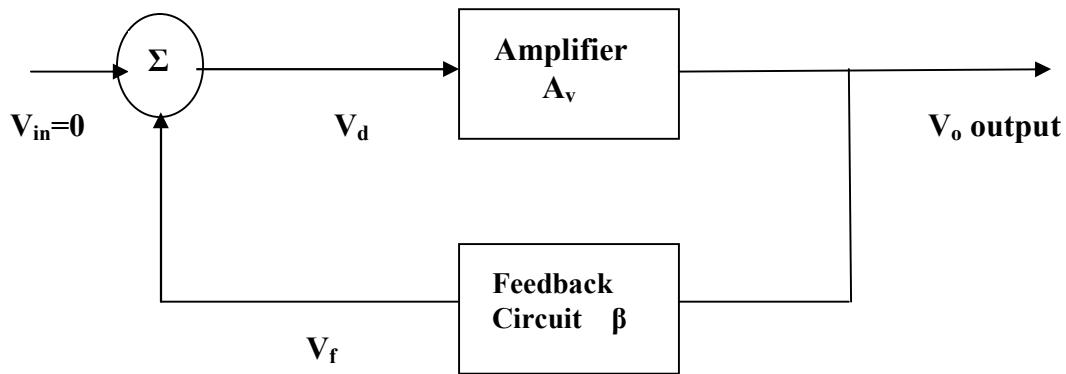


Figure.1

In the block diagram (Fig.1), $V_d = V_f + V_{in}$

$$V_o = A_v V_d \text{ and } V_f = \beta V_o$$

Using these relationships, following equation can be obtained:

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 - A_v \beta}$$

When $A_v \beta = 1$, $A_{fb} = \infty = \frac{V_o}{V_{in}}$, This will happen only when $V_{in} = 0$. That is we get a signal at output without any input. The condition $A_v \beta = 1$ is known as Barkhausen condition. This condition expressed in polar form as follows. $A_v \beta = 1 \angle 0^\circ \text{ or } 360^\circ$

Barkhausen condition gives two requirements for oscillation.

- 1) The magnitude of the loop gain must be equal to 1.
- 2) The total phase shift of the loop gain must be equal to $0^\circ \text{ or } 360^\circ$.

Phase shift Oscillator: Figure.2 gives the circuit diagram for a phase shift oscillator, which consists of an op-amp as the amplifying stage and three RC cascaded networks as the feedback circuit. The opamp used in this oscillator is in the inverting mode, output is 180° is phase shifted. To feedback the output to input, additional 180° degree phase shift is achieved by RC network.

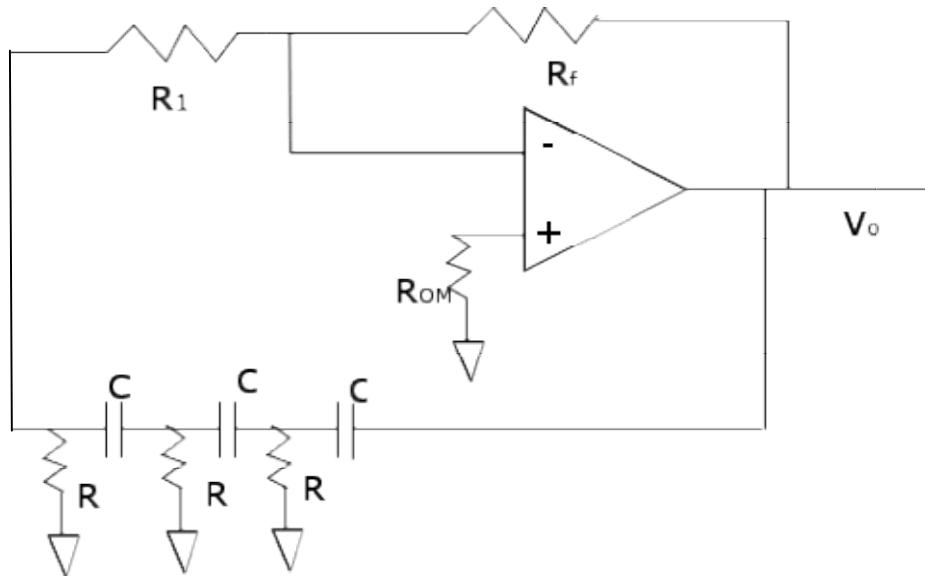


Figure.2

The frequency of oscillation is given by, $f = \frac{1}{2\pi\sqrt{6}RC}$ and at this frequency gain must be at least 29. That is $\left|\frac{R_f}{R_1}\right| = 29$.

Feedback circuit with RC network gives 180 degree phase shift but decreases the output voltage by a factor of 29. That is $\beta=1/29$. For the oscillations $A/\beta = 1$. Therefore, gain should be at least 29.

Procedure: Choose $R_f = 100 \text{ k}\Omega$, $R = 2 \text{ k}\Omega$, $C = 0.1 \text{ }\mu\text{F}$, $R=1 \text{ k}\Omega$ and construct a phase shift oscillator. Determine the oscillating frequency using oscilloscope and compare with calculated oscillation frequency.

Experimentally determine the minimum gain required to sustain oscillations by varying the gain in the circuit. Obtain Lissajous figure (circle) with X-Y mode of the oscilloscope and estimate oscillating frequency. Try to make the circuit for some other oscillating frequency by choosing components appropriately.

References: 1) OPAMPS and linear integrated circuits –Ramakant Gaykawad

2) <http://textofvideo.nptel.iitm.ac.in/122106025/lec35.pdf>

Lab#4 Digital Logic Families

Objective: To understand basic gate operation of following logic families:

- (i) Diode-Resistor Logic (DRL)
- (ii) Diode-Transistor Logic (DTL)
- (iii) Transistor-Transistor Logic (TTL)

Overview:

Digital Logic States

All digital electronic circuits and microprocessor based systems contain hardware elements called Digital Logic Gates that perform the logical operations of AND, OR and NOT on binary numbers. In digital logic only two voltage levels or states are allowed and these states are generally referred to as Logic "1" or Logic "0", High or Low, True or False and which are represented in *Boolean Algebra* and *Truth Tables* by the numbers "1" and "0" respectively. A good example of a digital logic level is a simple light as it is "ON" or "OFF".

Logic operations can be performed using any non-linear device that has at least two distinct regions of operation. Obvious choices for the electrical engineer are the semiconductor diode and the bipolar junction transistor. Particular voltage levels are assigned to logic levels 0 and 1.

While many voltage level assignments are possible, one common assignment is:

logic 1 (HIGH)----~ 5 V

logic 0 (LOW) ----~ 0 V.

This is known as "**Positive logic**" system. There is also a complementary "**Negative Logic**" system in which the values and the rules of a logic "0" and a logic "1" are reversed. But, unless stated otherwise, we shall only refer to the Positive Logic convention for all the experiments. It is important to note that noise, power source fluctuations, loading by other circuits, and other factors will cause the logic level voltages to vary over some range.

Simple Basic Digital Logic Gates

Simple digital logic gates can be made by combining transistors, diodes and resistors as discrete components. Let us investigate some of such circuits using Diode-Resistor Logic (DRL), Diode-Transistor Logic (DTL) and Transistor-Transistor Logic (TTL) as described below.

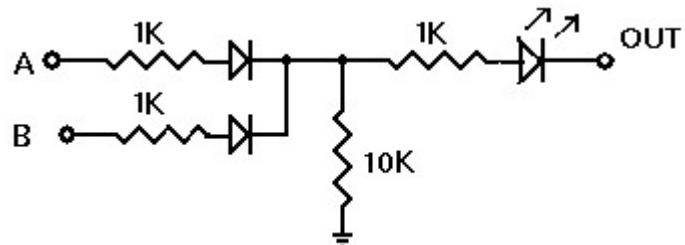
(i) Diode-Resistor Logic (DRL)

Diode logic gates use diodes to perform OR and AND logic functions as shown in the circuit diagram. Connection of the LED at the output is optional which simply displays the logical state of the output, i.e. the logic state of output is 0 or 1, if LED is off or on, respectively. Diodes have the property of easily passing an electrical current in one direction, but not the other. Thus, diodes can act as a logical switch. Diode logic gates are very simple and inexpensive, and can be used effectively in limited space. However, they cannot be used extensively due to the obvious logic level shift when gates are connected in series. In addition, they cannot perform a NOT function, so their usefulness is quite limited. This type of logic circuit is rarely found in integrated form.

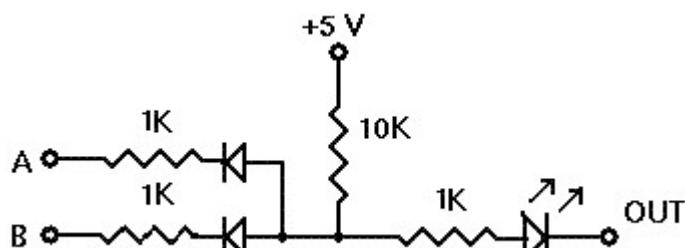
Circuit Components/Equipments:

1. Resistors (1K Ω , 3 Nos; 10K Ω , 1 No.)
2. 1N914 diodes or equivalent (2 Nos.)
3. A Surface mount dip switch
4. D.C. Power supply (5V)
5. A Red/Green LED
6. Connecting wires
7. Breadboard

Circuit Diagram:



DRL OR gate



DRL AND Gate

Procedure:

1. Assemble the circuit on your breadboard for OR/AND operation.
2. Turn on power to your experimental circuit.
3. Apply all four possible combinations of inputs at A and B from the power supply using dip switch.
4. For each input combination, note the logic state of the output, Q, as indicated by the LED (ON = 1; OFF = 0), and record that result in the table.
5. Compare your results with the truth table of a logic “OR”/ “AND” operation.
6. When you have completed your observations, turn off the power to your experimental circuit

Truth Tables:

Logic “OR” operation

| A | B | $Q = A+B$ |
|---|---|-----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Logic “AND” operation

| A | B | $Q = A.B$ |
|---|---|-----------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Observations:

(I) DRL OR gate:

| Input | | Output $Q = A+B$ |
|-------|---|---------------------|
| A | B | |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

(II) DRL AND gate:

| Input | | Output $Q = A.B$ |
|-------|---|---------------------|
| A | B | |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

Discussions:

Precautions:

(ii) Diode-Transistor Logic (DTL)

The simple 2-input Diode-Resistor gate can be converted into a NAND/NOR universal gate by the addition of a single transistor inverting (NOT) stage employing DTL. **Diode-Transistor Logic**, or **DTL**, refers to the technology for designing and fabricating digital circuits wherein logic gates employ diodes in the input stage and bipolar junction transistors at the output stage. The output BJT switches between its cut-off and saturation regions to create logic 1 and 0, respectively. The logic level shift problem of DRL gates is not present in DTL and TTL gates so that gates may be connected in series indefinitely. If a gate drives several similar gates in parallel problems may occur: the maximum number of gates that can be driven in parallel is identified as the "fanout" of a gate. DTL offers better noise margins and greater fan-outs than RTL (**Resistor- Transistor Logic**), but suffers from low speed, especially in comparison to TTL. Diodes take up far less room than resistors, and can be constructed easily. In addition, the internal resistance of a diode is small when the diode is forward biased, thus allowing for faster switching action. As a result, gates built with diodes in place of most resistors can operate at higher frequencies. Because of this diode-transistor logic (DTL) rapidly replaced RTL in most digital applications.

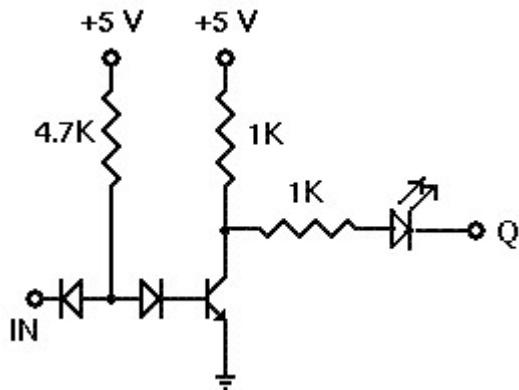
DTL Inverter Circuit

The DTL inverter uses a transistor and a collector load resistor as shown in the circuit diagram. The input is connected through a pair of diodes in series with the base of the transistor. The diode connected directly to the transistor base serves to raise the input voltage required to turn the transistor on to about 1.3 to 1.4 volts. Any input voltage below this threshold will hold the transistor off. The base resistor is also connected which should be sufficient to turn the transistor on and off quickly thus enabling higher switching speeds.

Circuit Components/Equipments:

1. Resistors (1K Ω 2 Nos., 4.7K Ω ; 1 No.)
2. 1N914/1N4148 silicon diodes (2 Nos.)
3. 2N4124 NPN silicon transistor (1 No.)
4. A Surface mount dip switch
5. D.C. Power supply (5V)
6. A Red/Green LED
7. Connecting wires
8. Breadboard

Circuit Diagram:



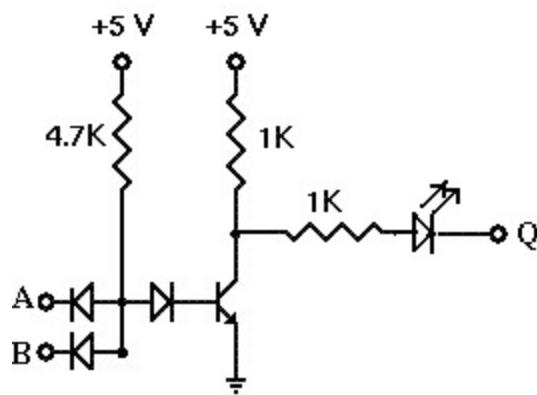
DTL NAND Circuit

The DTL NAND gate combines the DTL inverter with a simple Diode-Resistor Logic (DRL) AND gate as shown in its circuit diagram. Thus, any number of inputs can be added simply by adding input diodes to the circuit. The problem of signal degradation caused by Diode Logic is overcome by the transistor, which amplifies the signal while inverting it. This means DTL gates can be cascaded to any required extent, without losing the digital signal.

Circuit Components:

1. All the components from the DTL Inverter circuit
2. 1N914/1N4148 silicon diodes (1No., in addition to the previous two)

Circuit Diagram:



DTL NOR Circuit

Similar to DTL NAND circuit one can construct the NOR gate by using a DRL OR gate followed by a transistor inverter, as shown in circuit diagram (i). One can also construct a

DTL NOR more elegantly by combining multiple DTL inverters with a common output as shown in the schematic diagram (ii). Any number of inverters may be combined in this fashion to allow the required number of inputs to the NOR gate. (You should try both the circuits!)

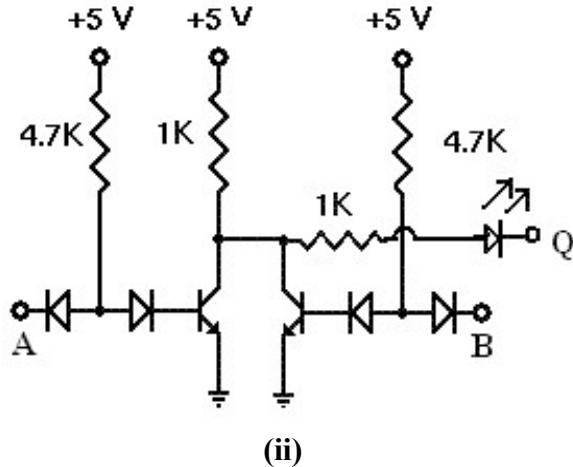
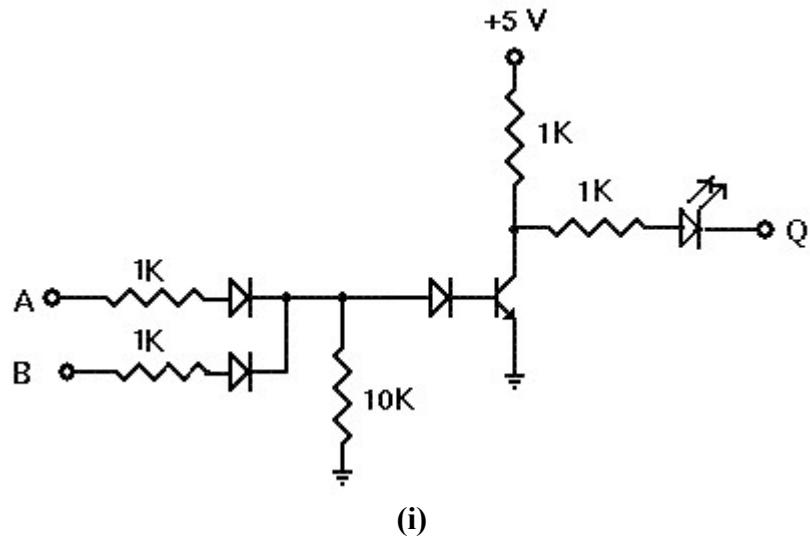
Circuit Components:

1. All the components from the DTL Inverter circuit, except power supply and $4.7\text{ K}\Omega$ resistor
2. 1N914/1N4148 silicon diodes (1No.,in addition to the previous two)

Or

1. All the components from the DTL Inverter circuit
2. 1N914/1N4148 silicon diodes (2Nos.,in addition to the previous two)
3. 2N4124 NPN silicon transistor (1No.,in addition to the previous one)

Circuit Diagram:



Procedure:

1. Assemble the circuit on your breadboard for NOT/NAND/NOR operation. First, start with the inverter circuit. Keep this circuit in tact after finishing the inverter experiment. The rest two circuits can be constructed by just adding extra components to the inverter circuit.
2. Turn on power to your experimental circuit.
3. Apply all four possible combinations of inputs at A and B from the power supply using dip switch.
4. For each input combination, note the logic state of the output, Q, as indicated by the LED (ON = 1; OFF = 0), and record that result in the table.
5. Compare your results with the truth table of a logic NOT/NAND/NOR operation.
6. When you have completed your observations, turn off the power supply.

Truth Tables:

Logic "NOT" operation

Logic "NOR" operation

Logic "NAND" operation

| A | Q = A' | A | B | Q = (A+B)' | A | B | Q = (A.B)' |
|----------|---------------|----------|----------|-------------------|----------|----------|-------------------|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| | | 1 | 0 | 0 | 1 | 0 | 1 |
| | | 1 | 1 | 0 | 1 | 1 | 0 |

Observations:

(I) DTL NOT gate:

| Input A | Output Q = A' |
|--------------------|--------------------------|
| 0 | |
| 1 | |

(II) DTL NOR gate:

| Input | | Output |
|--------------|----------|-------------------|
| A | B | Q = (A+B)' |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

(III) DTL NAND gate:

| Input | | Output |
|-------|---|--------------------|
| A | B | $Q = (A \cdot B)'$ |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

Discussions:

Precautions:

(iii) Transistor-Transistor Logic (TTL)

Transistor-transistor logic uses bipolar transistors in the input and output stages. TTL is commonly found in relatively low speed applications. Thus before using commercial ICs that uses TTL, let's first understand the circuit in discrete form.

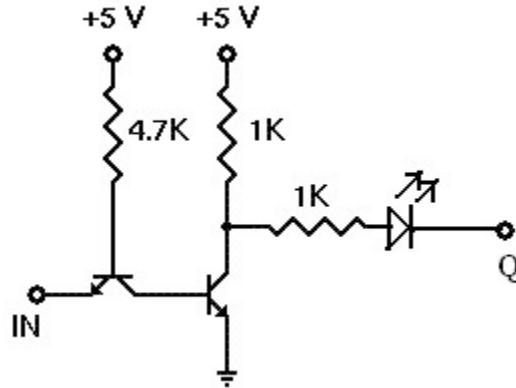
TTL Inverter Circuit

Looking at the DTL inverter circuit, one can note that the two diodes are opposed to each other in direction. That is, their P-type anodes are connected together and to the pull-up resistor, while one cathode is the signal input and the other is connected to the transistor's base. Thus, one can replace these two diodes with a single NPN transistor as shown in the circuit diagram. This makes lot of sense owing to the fact that the amount of space required by a transistor in an IC is essentially the same as the space required by a diode and by eliminating the space required by one diode at the same time.

Circuit Components/Equipments:

1. 2N4124 NPN silicon transistors (2 Nos.)
2. Resistors (1K Ω , 2 Nos.; 4.7K Ω 1 No.)
3. A Surface mount dip switch
4. D.C. Power supply (5V)
5. A Red/Green LED
6. Connecting wires
7. Breadboard

Circuit Diagram:



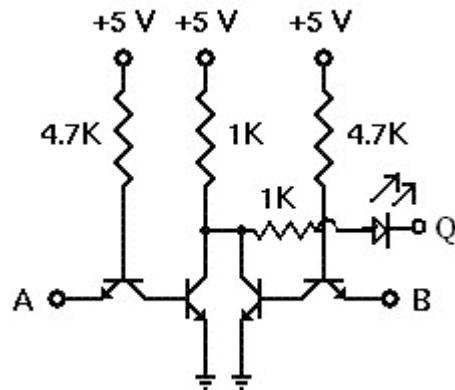
TTL NOR Circuit

TTL integrated circuits provide multiple inputs to NAND gates by designing transistors with multiple emitters on the chip. Unfortunately, we can't very well simulate that on a breadboard socket. However, a NOR gate can be designed using an extra inverter transistors just as in the case of DTL NOR gate.

Circuit Components/Equipments:

1. All the components of TTL inverter circuit
2. 2N4124 NPN silicon transistors (2Nos)
3. $4.7K\Omega$ resistor (1 No.)

Circuit Diagram:



Procedure:

1. Assemble the circuit on your breadboard for TTL NOT/NOR operation. First, start with the inverter circuit. Keep this circuit in tact to use it further in NOR circuit.

2. Turn on power to your experimental circuit. Apply all four possible combinations of inputs at A and B from the power supply using dip switch.
3. For each input combination, note the logic state of the output, Q, as indicated by the LED (ON = 1; OFF = 0), and record that result in the table.
4. Compare your results with the truth table of a logic NOT/NOR operation.
5. When you have completed your observations, turn off the power supply.

Truth Tables:

Logic “NOT” operation $A \quad Q = A'$

| | |
|---|---|
| 0 | 1 |
| 1 | 0 |

Logic “NOR” operation

$A \quad B \quad Q = (A+B)'$

| | | |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Observations:

(I) TTL NOT gate:

| Input A | Output $Q = A'$ |
|--------------------|---------------------------------------|
| 0 | |
| 1 | |

(II) TTL NOR gate:

| Input | | Output |
|--------------|----------|--------------------------------|
| A | B | $Q = (A+B)'$ |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

Discussions:

Precautions:

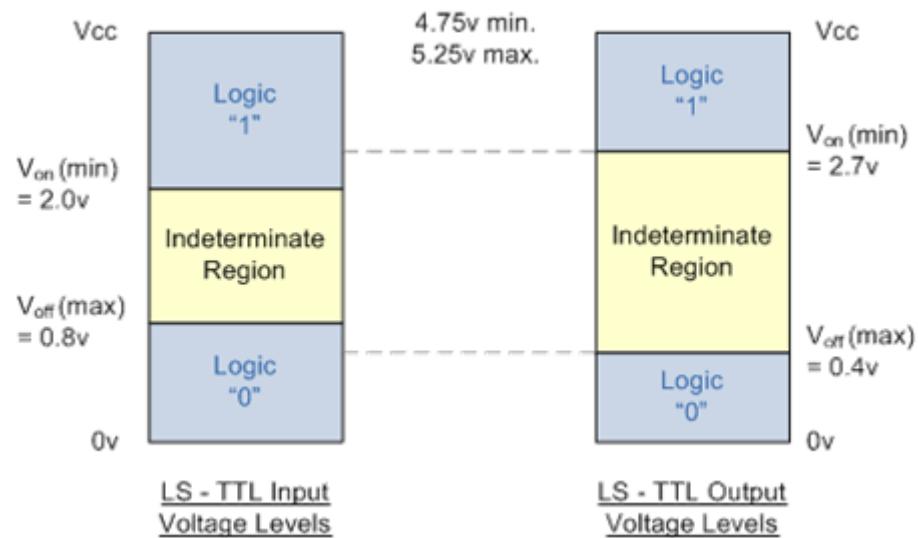
Lab#5: Study of Boolean Logic Operations using Digital ICs

Objective: To study and verify various Boolean logic operations and the De Morgan's laws using digital ICs.

Overview:

Standard commercially available **Digital Logic Gates** are available in two basic forms, **TTL** which stands for *Transistor-Transistor Logic* such as the 7400 series, and **CMOS** which stands for *Complementary Metal-Oxide-Silicon* which is the 4000 series of Integrated Circuits, (IC) or "chips" as it is commonly called. Generally speaking, **TTL** IC's use NPN type *Bipolar Junction Transistors* while **CMOS** IC's use *Field Effect Transistors* or FET's for both their input and output circuitry.

There are a large variety of logic gate types in both the Bipolar and CMOS families of digital logic gates such as 74L, 74LS, 74ALS, 74HC, 74HCT, 74ACT etc, with each one having its own distinct advantages and disadvantages and the exact voltages required to produce a logic "0" or logic "1" depends upon the specific logic group or family. However, when using a standard +5 volt supply any TTL voltage input between 2.0V and 5V is considered to be a logic "1" or "HIGH" while any voltage input below 0.8v is recognized as a logic "0" or "LOW". TTL outputs are typically restricted to narrower limits of between 0 V and 0.4 V for a "low" and between 2.7 V and 5 V. The voltage region between the maximum voltage of logic "0" and minimum voltage of logic "1" of either input or output is called the *Indeterminate Region*. CMOS logic uses a different level of voltages with a logic "1" level operating between 3 and 15 volts.



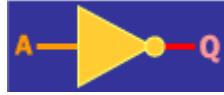
TTL Input & Output Voltage Levels

There are several simple gates that you need to learn about. With these simple gates you can build combinations that will implement any digital component you can imagine.

- The simplest possible gate is called an "inverter," or a **NOT gate**. It takes one bit as input and produces output as its opposite. The logic table for NOT gate and its symbol are shown below.

NOT Gate

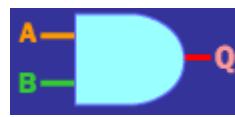
| A | Q |
|---|---|
| 0 | 1 |
| 1 | 0 |



- The **AND gate** performs a logical "and" operation on two inputs, A and B:

AND Gate

| A | B | Q |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



- The **OR gate** performs a logical "or" operation on two inputs, A and B:

OR Gate

| A | B | Q |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



- It is quite common to recognize two others as well: the **NAND** and the **NOR** gate. These two gates are simply combinations of an AND or an OR gate with a NOT gate.

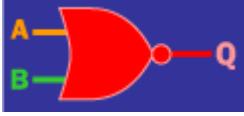
NAND Gate

| A | B | Q |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



NOR Gate

| A | B | Q |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |



- The final two gates that are sometimes added to the list are the **XOR** and **XNOR** gates, also known as "exclusive or" and "exclusive nor" gates, respectively. Here are their tables:

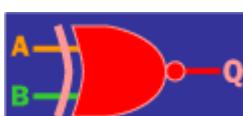
XOR Gate

| A | B | Q |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



XNOR Gate

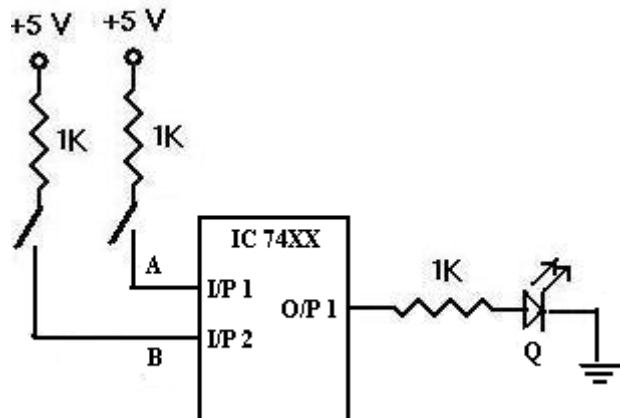
| A | B | Q |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



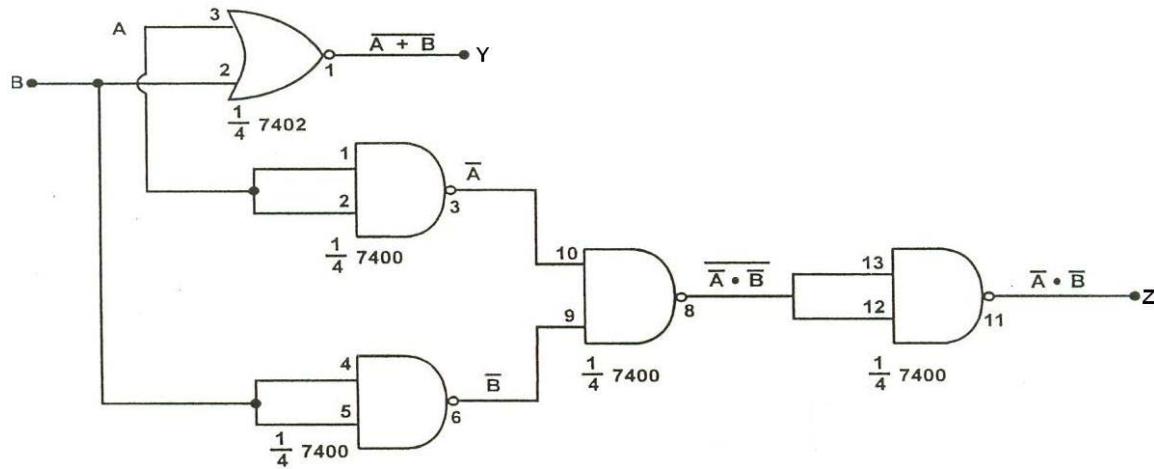
Circuit Components/Equipments:

- Digital ICs,
- Resistors,
- DIP switch,
- D.C. Power supply (5V),
- LEDs,
- Breadboard,
- Connecting wires.

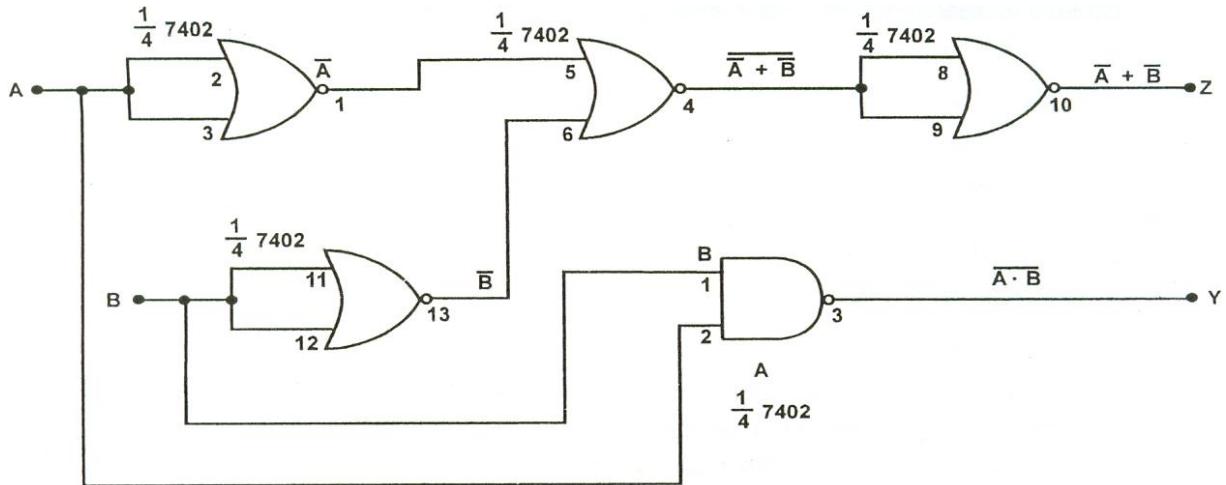
Circuit Diagrams: (in general, for all ICs)



De Morgan's law: $(\overline{A} + \overline{B}) = \overline{A} \cdot \overline{B}$



De Morgan's law: $(A \cdot B)' = \overline{A} + \overline{B}$



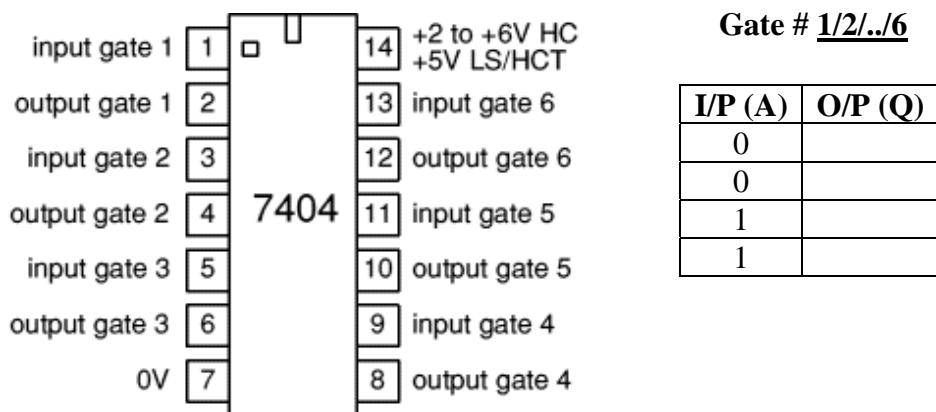
Procedure:

1. Place the IC on the breadboard.
2. Connect pin 14 (V_{CC}) to 5V and pin 7 (ground) to 0V terminal of the power supply.
3. Following the general circuit diagram facilitate all possible combinations of inputs from the power supply, using dip switch and resistors. Connect the output pin to ground through a resistor and LED.
4. Turn on power to your experimental circuit.
5. For each input combination, note the logic state of the outputs as indicated by the LEDs (ON = 1; OFF = 0), and record the result in the table.
6. Compare your results with the truth table for operation.

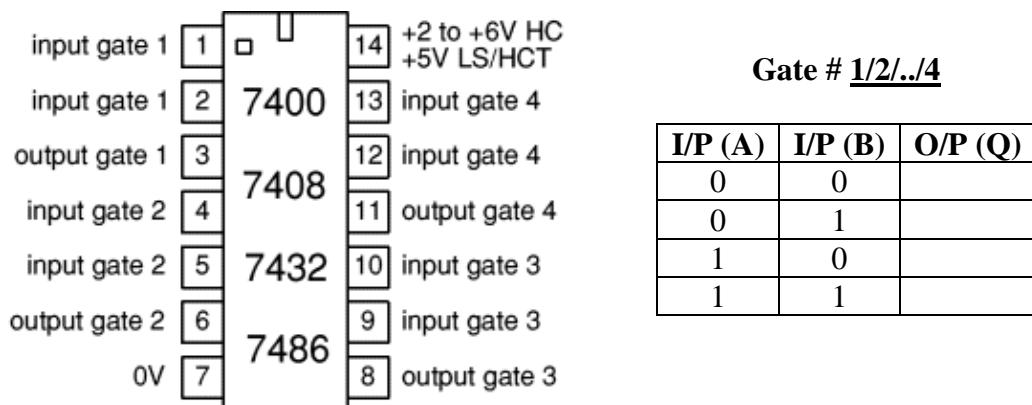
7. For verification of De Morgan's laws, follow the respective circuit diagrams using appropriate ICs. Follow the general circuit diagram for connections for input and output using dip switch and LEDs.
8. Monitor the outputs Y and Z using LEDs and confirm that Y and Z are the same for any states of A and B.
9. When you are done, turn off the power to your experimental circuit.

Observations: Verification of Boolean Logic Operations

(I) Inverter gate (NOT): IC 7404LS



(II) 2-input AND gate: IC 7408LS



(III) 2-input OR gate: IC 7432LS

Gate # 1/2/../4

| I/P (A) | I/P (B) | O/P (Q) |
|---------|---------|---------|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

(IV) 2-input EX-OR gate: IC 7486LS

Gate # 1/2/../4

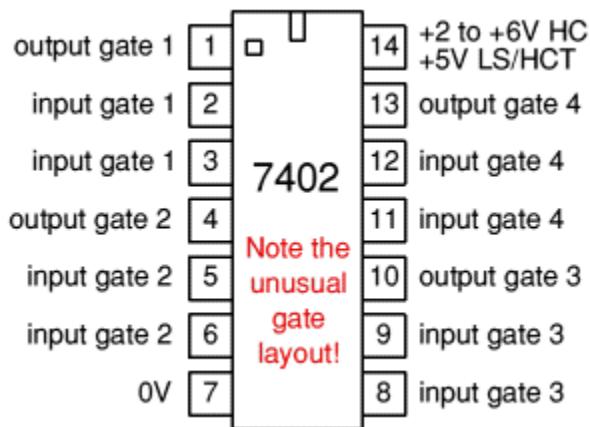
| I/P (A) | I/P (B) | O/P (Q) |
|---------|---------|---------|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

(V) 2-input NAND gate: IC 7400LS

Gate # 1/2/../4

| I/P (A) | I/P (B) | O/P (Q) |
|---------|---------|---------|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

(VI) 2-input NOR gate: IC 7402LS



Gate # 1/2/../4

| I/P (A) | I/P (B) | O/P (Q) |
|---------|---------|---------|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

Verification of De Morgan's laws:

$$\overline{(A + B)} = \overline{A} \cdot \overline{B}$$

| I/P (A) | I/P (B) | $\overline{(A + B)}$ | Y(Observed) | \overline{A} | \overline{B} | $\overline{A} \cdot \overline{B}$ | Z(Observed) |
|---------|---------|----------------------|-------------|----------------|----------------|-----------------------------------|-------------|
| 0 | 0 | | | | | | |
| 0 | 1 | | | | | | |
| 1 | 0 | | | | | | |
| 1 | 1 | | | | | | |

$$(\overline{A \cdot B}) = \overline{A} + \overline{B}$$

| I/P (A) | I/P (B) | (A · B) | Y(Observed) | \overline{A} | \overline{B} | $\overline{A} + \overline{B}$ | Z(Observed) |
|---------|---------|---------|-------------|----------------|----------------|-------------------------------|-------------|
| 0 | 0 | | | | | | |
| 0 | 1 | | | | | | |
| 1 | 0 | | | | | | |
| 1 | 1 | | | | | | |

Discussions:

Precautions:

Lab#6: Study of Adder and Subtractor Circuits

Objective:

- (i) To construct half and full adder circuit and verify its working
- (ii) To construct half and full subtractor circuit and verify its working
- (iii) To construct a full adder-subtractor circuit

Overview:

Half adder:

Let's start with a **half (single-bit) adder** where you need to add single bits together and get the answer. The way you would start designing a circuit for that is to first look at all of the logical combinations. You might do that by looking at the following four sums:

$$\begin{array}{r} 0 \quad 0 \quad 1 \quad 1 \\ + 0 \quad + 1 \quad + 0 \quad + 1 \\ \hline 0 \quad 1 \quad 1 \quad 10 \end{array}$$

That looks fine until you get to $1 + 1$. In that case, you have a **carry bit** to worry about. If you don't care about carrying (because this is, after all, a 1-bit addition problem), then you can see that you can solve this problem with an XOR gate. But if you do care, then you might rewrite your equations to always include **2 bits of output**, like this:

$$\begin{array}{r} 0 \quad 0 \quad 1 \quad 1 \\ + 0 \quad + 1 \quad + 0 \quad + 1 \\ \hline 00 \quad 01 \quad 01 \quad 10 \end{array}$$

Now you can form the logic table:

1-bit Adder with Carry-Out

| A | B | Q | C |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

By looking at this table you can see that you can implement the sum Q with an XOR gate and C (carry-out) with an AND gate.

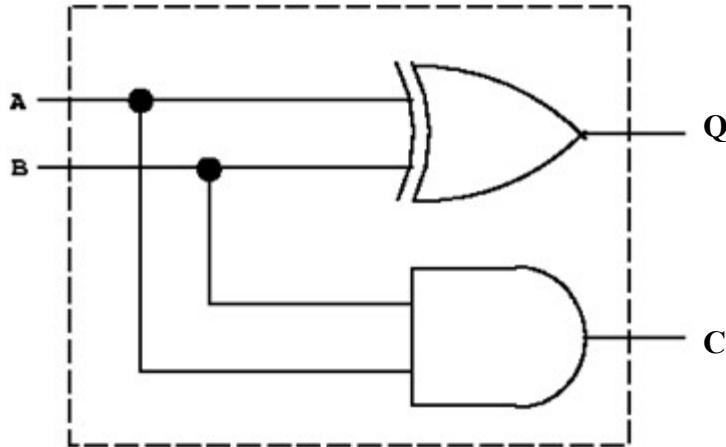


Fig. 1: Schematics for half adder circuit

Full adder:

If you want to add two or more bits together it becomes slightly harder. In this case, we need to create a full adder circuits. The difference between a full adder and a half adder we looked at is that a full adder accepts inputs A and B plus a **carry-in** (C_{N-1}) giving outputs Q and C_N . Once we have a full adder, then we can string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next. The logic table for a full adder is slightly more complicated than the tables we have used before, because now we have **3 input bits**. The truth table and the circuit diagram for a full-adder is shown in Fig. 2. If you look at the Q bit, it is 1 if an odd number of the three inputs is one, i.e., Q is the XOR of the three inputs. The full adder can be realized as shown below. Notice that the full adder can be constructed from two half adders and an **OR** gate.

One-bit Full Adder with Carry-In & Carry-Out

| C_{N-1} | A | B | Q | C_N |
|-----------|---|---|---|-------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

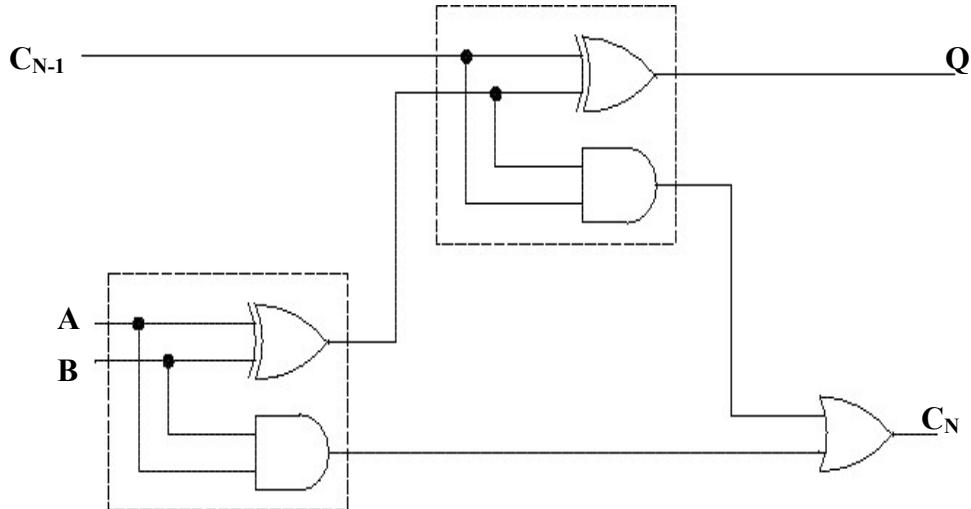


Fig. 2: Truth table and schematics for full adder circuit

Now we have a piece of functionality called a "full adder", which can be combined with a half adder to construct a 2-bit adder. Adders for arbitrarily large (say N -bit) binary numbers can be constructed by cascading full adders. These are called a **ripple-carry** adder, since the carry bit "ripples" from one stage to the next. The schematics for a 4-bit full adder circuit is shown below. This implementation has the advantage of simplicity but the disadvantage of speed problems. In a real circuit, gates take time to switch states (the time is of the order of nanoseconds, but in high-speed computers nanoseconds matter). So 32-bit or 64-bit ripple-carry adders might take 100 to 200 nanoseconds to settle into their final sum because of carry ripple.

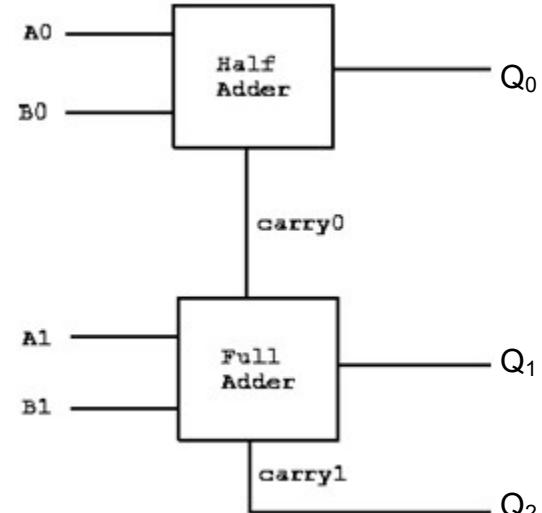


Fig. 3: Schematics of 2-bit adder

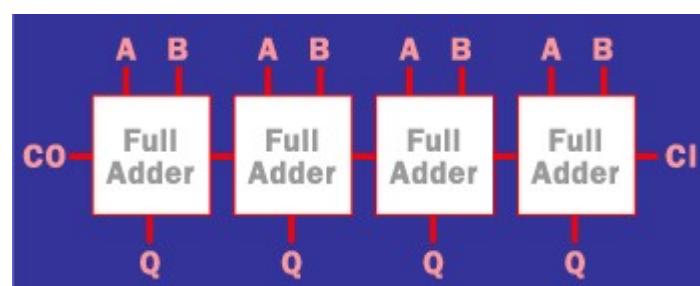


Fig.4: Schematics of 4-bit adder

Subtraction:

In a similar fashion subtraction can be performed using binary numbers. The truth table for a single bit or half-subtractor with inputs A and B is given below along with its circuit diagram (Fig.5). A full subtractor circuit accepts a minuend (A) and the subtrahend (B) and a borrow (B_{IN}) as inputs from a previous circuit. A full subtractor circuit can be realized by combining two half subtractor circuits and an OR gate as shown in Fig. 6.

1-bit Subtractor with Borrow

| A | B | Q | B _{IN} |
|---|---|---|-----------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

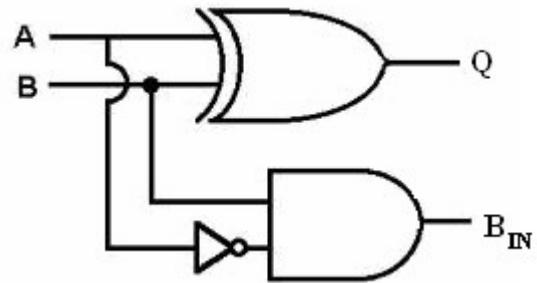


Fig. 5: Truth table and schematics for half subtractor circuit

1-bit Full Subtractor with B_{N-1}& B_N

| B _{N-1} | A | B | Q | B _N |
|------------------|---|---|---|----------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

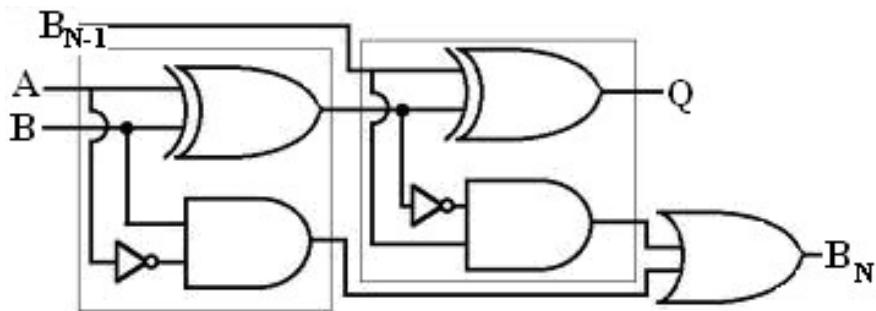


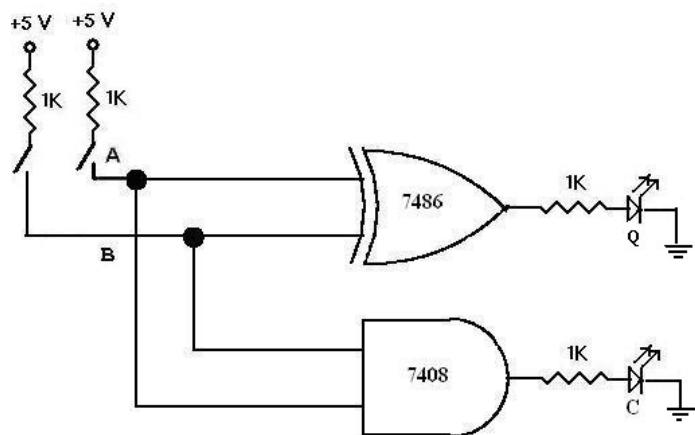
Fig. 6: Truth table and schematics for full subtractor circuit

However, it is possible to use the same circuit to perform addition and subtraction by replacing the ‘NOT’ gate of the subtractor circuit by an ‘XOR’ as shown in the circuit diagram below. Here, the second input (first input is from supply) for XOR gate decides the function of the circuit, i.e. addition or subtraction. This means if the second input for XOR is 0, the circuit will do addition and if 1, it will do subtraction.

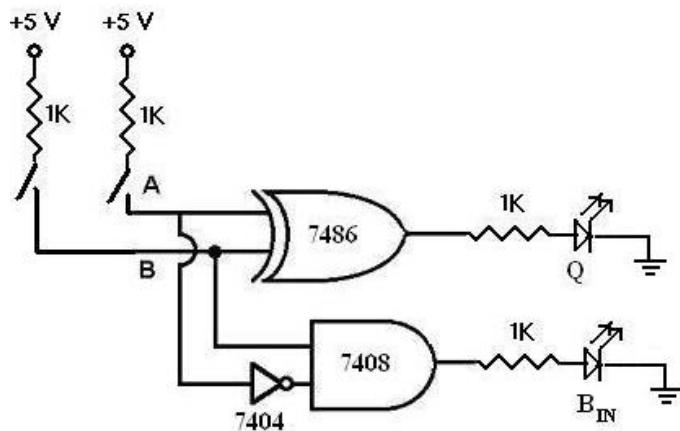
Circuit components/Equipments:

1. Resistors (1KΩ, 5 Nos)
2. ICs (XOR-7486, AND-7408, OR-7432, NOT-7404,)
3. A Surface mount dip switch
4. D.C. Power supply (5V)
5. Red/Green LEDs (2 Nos)
6. Connecting wires
7. Breadboard

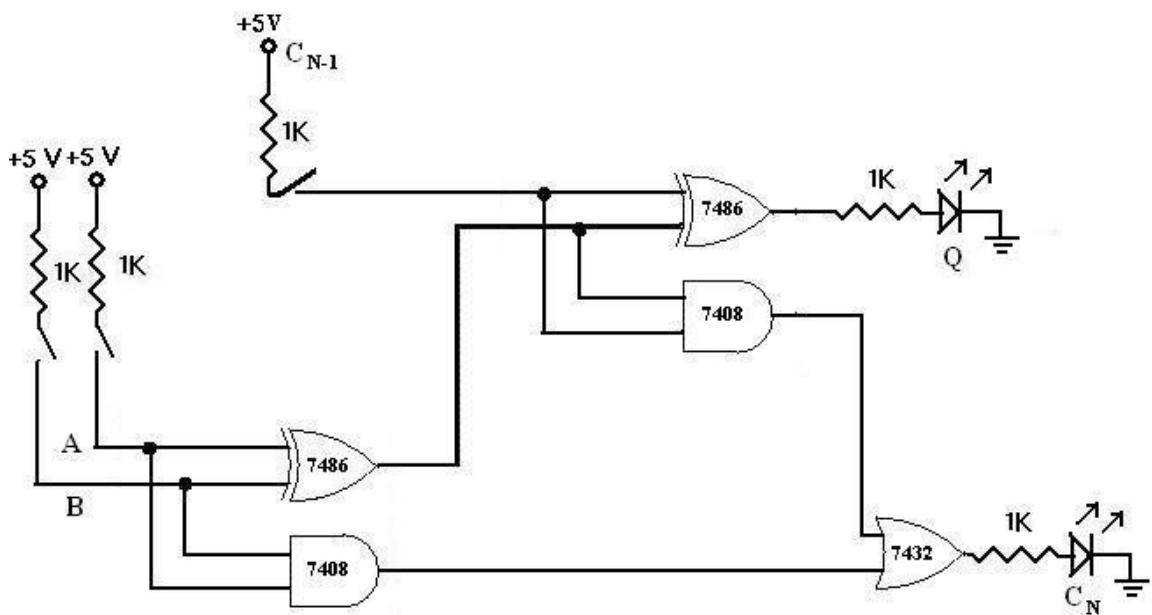
Circuit Diagrams:



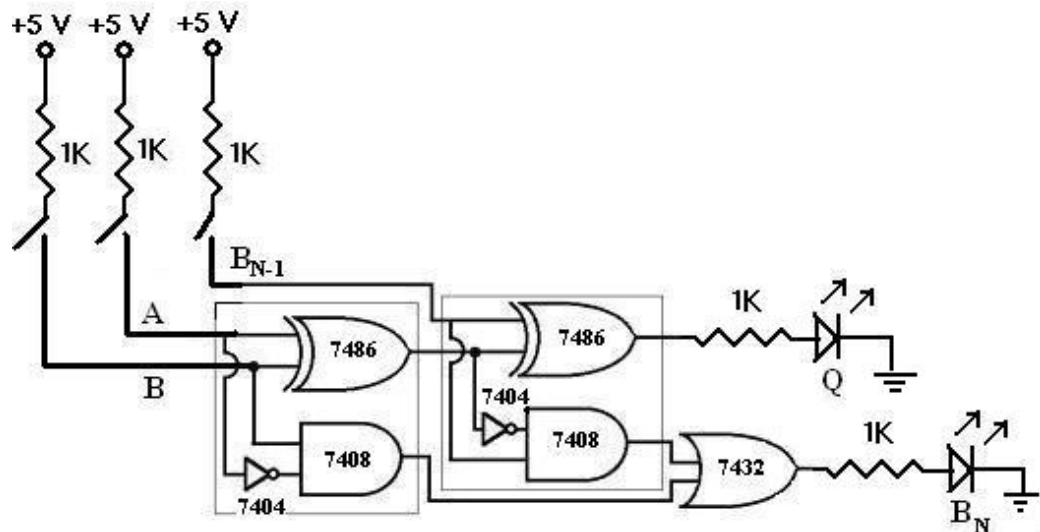
Half Adder



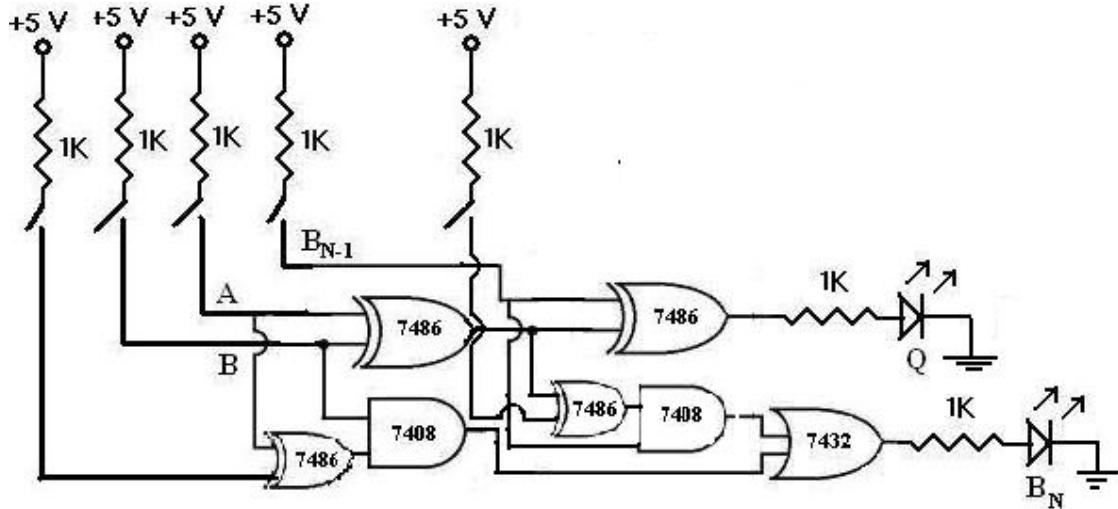
Half Subtractor



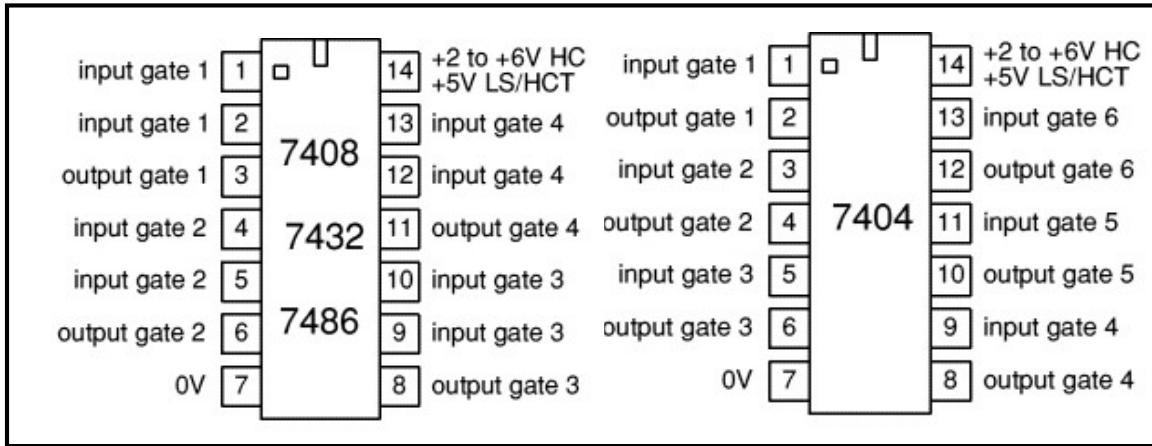
Full Adder



Full Subtractor



Full Adder-Subtractor



Schematics for detailed pin connections for different ICs

Procedure:

1. Assemble the circuits one after another on your breadboard as per the circuit diagrams.
2. Connect the ICs properly to power supply (pin 14) and ground (pin 7) following the schematics for different ICs shown above.
3. Using dip switch and resistors, facilitate all possible combinations of inputs from the power supply.
4. Turn on power to your experimental circuit.
5. For each input combination, note the logic state of the outputs as indicated by the LEDs (ON = 1; OFF = 0), and record the result in the table.
6. Compare your results with the truth table for operation.
7. When you are done, turn off the power to your experimental circuit.

Lab # 7: Study of Various Flip-Flop Circuits

Objective:

To construct and study the operations of the following circuits:

- (i) RS and Clocked RS Flip-Flop
- (ii) D Flip-Flop
- (iii) JK and Master-Slave JK Flip-Flop
- (iv) T Flip-Flop

Overview:

So far you have encountered with *combinatorial logic*, i.e. circuits for which the output depends only on the inputs. In many instances it is desirable to have the next output depending on the current output. A simple example is a *counter*, where the next number to be output is determined by the current number stored. Circuits that remember their current output or state are often called *sequential logic* circuits. Clearly, sequential logic requires the ability to store the current state. In other words, *memory* is required by sequential logic circuits, which can be created with boolean gates. If you arrange the gates correctly, they will remember an input value. This simple concept is the basis of RAM (random access memory) in computers, and also makes it possible to create a wide variety of other useful circuits.

Memory relies on a concept called **feedback**. That is, the output of a gate is fed back into the input. The simplest possible feedback circuit using two inverters is shown below (Fig.1):



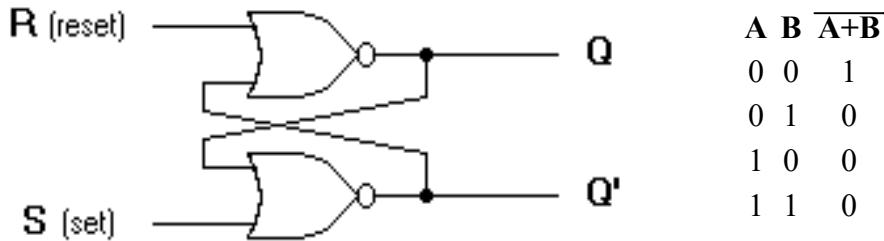
Fig.1: Simplest realization of feedback circuit

If you follow the feedback path, you can see that if Q happens to be 1 (or 0), it will always be 1 (or 0). Since it's nice to be able to control the circuits we create, this one doesn't have much use -- but it does let you see how feedback works. It turns out that in "real" sequential circuits, you can actually use this sort of simple inverter feedback approach. The memory elements in these circuits are called *flip-flops*. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter a flip-flop in a variety of ways and gives rise to different types of flip-flops.

RS Flip-Flop

RS flip-flop is the simplest possible memory element. It can be constructed from two NAND gates or two NOR gates. Let us understand the operation of the RS flip-flop using NOR gates as shown below using the truth table for ‘A NOR B’ gate. The inputs R and S are referred to as the Reset and Set inputs, respectively. The outputs Q and Q' are complements of each other and are referred to as the normal and complement outputs, respectively. The binary state of the flip-flop is taken to be the value of the normal output. When Q=1 and Q'=0, it is in the *set state* (or 1-state). When Q=0 and Q'=1, it is in the *reset/clear state* (or 0-state).

Circuit Diagram:



- **S=1 and R=0:** The output of the bottom NOR gate is equal to zero, $Q'=0$. Hence both inputs to the top NOR gate are equal to 0, thus, $Q=1$. Hence, the input combination S=1 and R=0 leads to the flip-flop being **set** to $Q=1$.
- **S=0 and R=1:** Similar to the arguments above, the outputs become $Q=0$ and $Q'=1$. We say that the flip-flop is **reset**.
- **S=0 and R=0:** Assume the flip-flop was previously in set (S=1 and R=0) condition. Now changing S to 0 results Q' still at 0 and $Q=1$. Similarly, when the flip-flop was previously in a reset state (S=0 and R=1), the outputs do not change. Therefore, with inputs S=0 and R=0, the flip-flop holds its state.
- **S=1 and R=1:** This condition violates the fact that both outputs are complements of each other since each of them tries to go to 0, which is not a stable configuration. It is impossible to predict which output will go to 1 and which will stay at 0. In normal operation this condition must be avoided by making sure that 1's are not applied to both inputs simultaneously, thus making it one of the main disadvantages of RS flip-flop.

All the above conditions are summarized in the characteristic table below:

Characteristic Table:

| R | S | Q | Q' | Comment |
|---|---|---|----|---------------|
| 0 | 0 | Q | Q' | Hold state |
| 0 | 1 | 1 | 0 | Set |
| 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | ? | ? | Indeterminate |

Debounce circuit

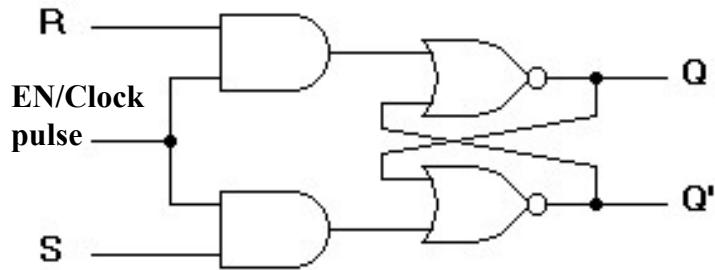
An elementary example using this flip-flop is the debounce circuit. Suppose a piece of electronics is to change state under the action of a mechanical switch. When this switch is moved from position S to R ($S=0, R=1$), the contacts make and break several times at R before settling to good contact. It is desirable that the electronics should respond to the first contact and then remain stable, rather than switching back and forth as the circuit makes and breaks. This is achieved by RS flip-flop which is reset to $Q=0$ by the first signal $R=1$ and remains in a fixed state until the switch is moved back to position S, when the signal $S=1$ sets the flip-flop to $Q=1$.

Gated or Clocked RS Flip-Flop

It is sometimes desirable in sequential logic circuits to have a bistable RS flip-flop that only changes state when certain conditions are met regardless of the condition of either the Set or the Reset inputs. By connecting a 2-input AND gate in series with each input terminal of the RS NOR Flip-flop a Gated RS Flip-flop can be created. This extra conditional input is called an "Enable" input and is given the prefix of "EN" as shown below. When the Enable input "EN" = 0, the outputs of the two AND gates are also at logic level 0, (AND Gate principles) regardless of the condition of the two inputs S and R, latching the two outputs Q and Q' into their last known state. When the enable input "EN" = 1, the circuit responds as a normal RS bistable flip-flop with the two AND gates becoming transparent to the Set and Reset signals. This Enable input can also be connected to a clock timing signal adding clock synchronisation to the flip-flop creating what is sometimes called a "Clocked SR Flip-flop".

So a **Gated/Clocked RS Flip-flop** operates as a standard bistable latch but the outputs are only activated when a logic "1" is applied to its EN input and deactivated by a logic "0". The property of this flip-flop is summarized in its characteristic table where Q_n is the logic state of the previous output and Q_{n+1} is that of the next output and the clock input being at logic 1 for all the R and S input combinations.

Circuit Diagram:



Characteristic Table:

| Q_n | R | S | Q_{n+1} |
|-------|---|---|---------------|
| 0 | 0 | 0 | 0 (Hold) |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | Indeterminate |
| 1 | 0 | 0 | 1 (Hold) |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | Indeterminate |

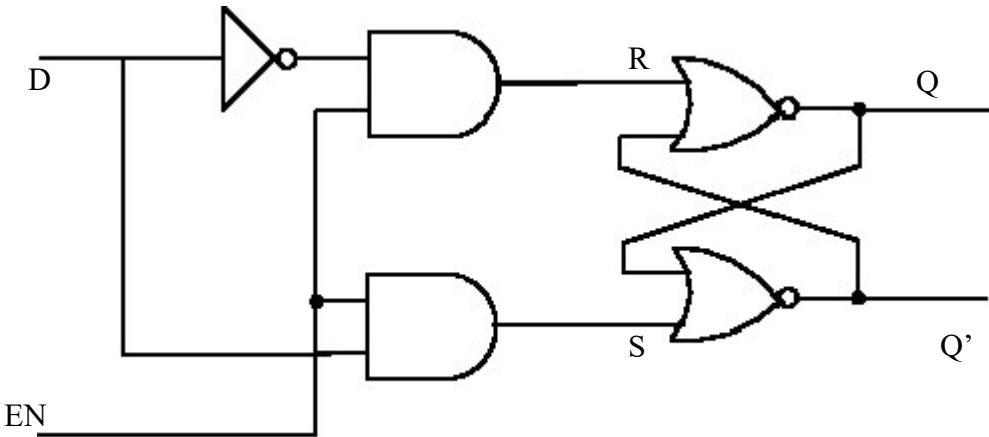
D FLIP-FLOP

An RS flip-flop is rarely used in actual sequential logic because of its undefined outputs for inputs $R = S = 1$. It can be modified to form a more useful circuit called D flip-flop, where D stands for data. The D flip-flop has only a single data input D as shown in the circuit diagram. That data input is connected to the S input of an RS flip-flop, while the inverse of D is connected to the R input. To allow the flip-flop to be in a holding state, a D-flip flop has a second input called Enable, EN. The Enable-input is AND-ed with the D-input.

- When **EN=0**, irrespective of D-input, the $R = S = 0$ and the **state is held**.
- When **EN= 1**, the S input of the RS flip-flop equals the D input and R is the inverse of D. Hence, output **Q follows D**, when EN= 1.
- When **EN returns to 0**, the most recent input **D is ‘remembered’**.

The circuit operation is summarized in the characteristic table for **EN=1**.

Circuit Diagram:



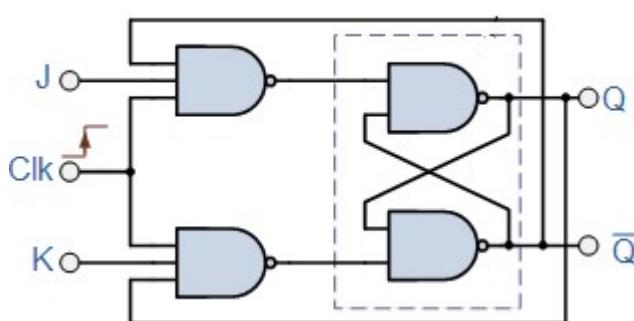
Characteristic Table:

| Q_n | D | Q_{n+1} |
|-------|-----|-----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

JK FLIP-FLOP:

The JK flip flop (JK means Jack Kilby, a Texas instrument engineer, who invented it) is the most versatile flip-flop, and the most commonly used flip flop. Like the RS flip-flop, it has two data inputs, J and K, and an EN/clock pulse input (CP). Note that in the following circuit diagram NAND gates are used instead of NOR gates. It has no undefined states, however. The fundamental difference of this device is the feedback paths to the AND gates of the input, i.e. Q is AND-ed with K and CP and \bar{Q} with J and CP.

Circuit Diagram:



Characteristic Table:

| Q_n | J | K | Q_{n+1} |
|-------|-----|-----|-------------------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1(Toggle, \bar{Q}_n) |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0(Toggle, \bar{Q}_n) |

The JK flip-flop has the following characteristics:

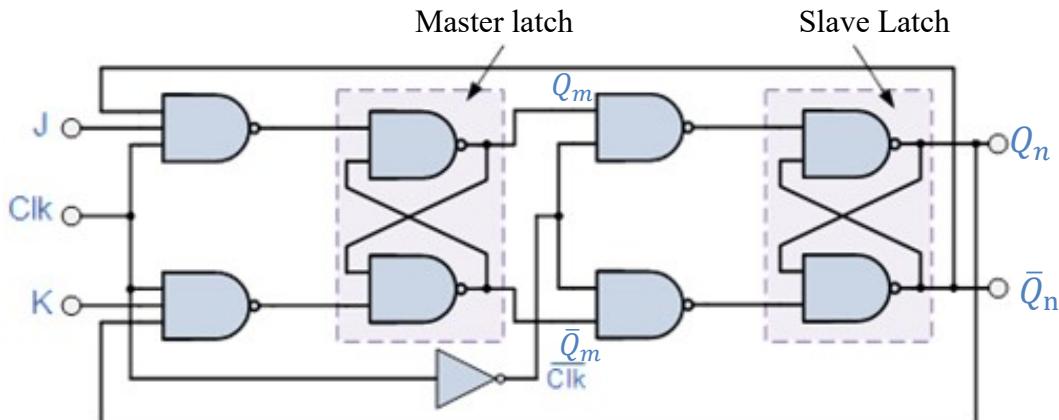
- If one input (J or K) is at logic 0, and the other is at logic 1, then the output is set or reset (by J and K respectively), just like the RS flip-flop.
- If both inputs are 0, then it remains in the same state as it was before the clock pulse occurred; again like the RS flip flop. CP has no effect on the output.
- If both inputs are high, however the flip-flop changes state whenever a clock pulse occurs; i.e., the clock pulse toggles the flip-flop again and again until the CP goes back to 0 as shown in the shaded rows of the characteristic table above. Since this condition is undesirable, it should be eliminated by an improvised form of this flip-flop as discussed in the next section.

MASTER-SLAVE JK FLIP-FLOP:

Although JK flip-flop is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race" if the output Q changes state before the timing pulse of the clock input has time to go "OFF", so the timing pulse period (T) must be kept as short as possible (high frequency). As this is sometimes not possible with modern TTL IC's the much improved Master-Slave J-K Flip-Flop was developed. This eliminates all the timing problems by using two SR flip-flops connected together in series, one for the "Master" circuit, which triggers on the leading edge of the clock pulse and the other, the "Slave" circuit, which triggers on the falling edge of the clock pulse.

The master-slave JK flip flop consists of two flip flops arranged so that when the clock pulse enables the first, or master, it disables the second, or slave. When the clock changes state again (i.e., on its falling edge) the output of the master latch is transferred to the slave latch. Again, toggling is accomplished by the connection of the output with the input AND gates.

Circuit Diagram:



Characteristic Table:

| CP | J | K | Q_m | \bar{Q}_m | Q_n | \bar{Q}_n |
|-----|---|---|-------|-------------|-------|-------------|
| 0→1 | 0 | 0 | | Hold | | Hold |
| 1→0 | 0 | 0 | | Hold | | Hold |
| 0→1 | 0 | 1 | 0 | 1 | | Hold |
| 1→0 | 0 | 1 | | Hold | 0 | 1 |
| 0→1 | 1 | 0 | 1 | 0 | | Hold |
| 1→0 | 1 | 0 | | Hold | 1 | 0 |
| 0→1 | 1 | 1 | | Toggle | | Hold |
| 1→0 | 1 | 1 | | Hold | | Toggle |

T FLIP-FLOP:

The T flip-flop is a single input version of the JK flip-flop. The T flip-flop is obtained from the JK type if both inputs are tied together.

Circuit Diagram:

Same as Master-Slave JK flip-flop with $J=K=1$

- The toggle, or T, flip-flop is a bistable device, where the output of the T flip-flop "toggles" with each clock pulse.
- Till $CP=0$, the output is in hold state (three input AND gate principle).
- When $CP=1$, for $T=0$, previous output is memorized by the circuit. When $T=1$ along with the clock pulse, the output toggles from the previous value as given in the characteristic table below.

Characteristic Table:

| Q_n | T | Q_{n+1} |
|-------|---|-----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Circuit components/Equipments:

1. Resistors (1KΩ, 5 Nos)
2. ICs [NOR-7402, AND(2-input)-7408, NAND(3-input)-7410, NAND-7400, NOT-7404]
3. A Surface mount dip switch
4. D.C. Power supply (5V)
5. Red/Green LEDs (4 Nos)
6. Connecting wires
7. Breadboard

Circuit Diagrams:

Already provided with text.

Procedure:

1. Assemble the circuits one after another on your breadboard as per the circuit diagrams. Circuit diagrams given here do not show connections to power supply and LEDs assuming that you are already familiar with it from your previous lab experience.
2. Connect the ICs properly to power supply (pin 14) and ground (pin 7) following the schematics for ICs given above.
3. Using dip switch and resistors, facilitate all possible combinations of inputs from the power supply. Use the switch also to facilitate pulse input to the circuit.
4. Turn on power to your experimental circuit.
5. For each input combination, note the logic state of the normal and complementary outputs as indicated by the LEDs (ON = 1; OFF = 0), and record the results in a table.
6. Compare your results with the characteristic tables.
7. When you are done, turn off the power to your experimental circuit.

Observations:

Table For RS FF: _____

Table For Gated RS FF: _____

Table For D FF: _____

Table For JK FF: _____

Table For Master-Slave JK FF: _____

Table For T FF: _____

Discussions:

Precautions:

1. Watch out for loose connections.
2. While changing the input condition keep the dip switch well pressed.

Lab # 8: Study of Counter Circuits

Objectives: To construct and study the operations of the following circuits:

- (i) A 4-bit binary ripple Up-counter
- (ii) A 4-bit binary ripple Down-counter
- (iii) A Mod-12 counter
- (iv) A Ring counter

Overview:

Binary Counters are one of the applications of sequential logic using flip-flops. A counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, in form of a clock pulse. Counters can be formed by connecting individual flip-flops together. On application of pulses, the flip-flops in the counter undergo a change of state in such a manner that the binary number stored in the flip-flops represents the number of pulses applied at input. When clock pulses are applied to a counter, the counter progresses from one state to another and the final output of the flip-flop in the counter indicates the pulse count. If all the flip-flops are not clocked at the same time, the counter is *asynchronous (or Ripple)* and if they are clocked simultaneously, the counter is *synchronous*. In practice, there are two types of counters:

- up counters, for increment in value
- down counters, for decrement in value

Frequency Division: For frequency division, toggle mode flip-flops are used in a chain as a divide by two- counter. One flip-flop will divide the input clock frequency by 2, two flip-flops will divide it by 4 (and so on). One benefit of using toggle flip-flops for frequency division is that the output at any point has an exact 50% duty cycle. The final output clock signal will have a frequency value equal to the input clock frequency divided by the MOD number of the counter. Such circuits are known as "divide-by-n" counters, where "n" is the number of counter stages used.

Binary ripple Up-counter:

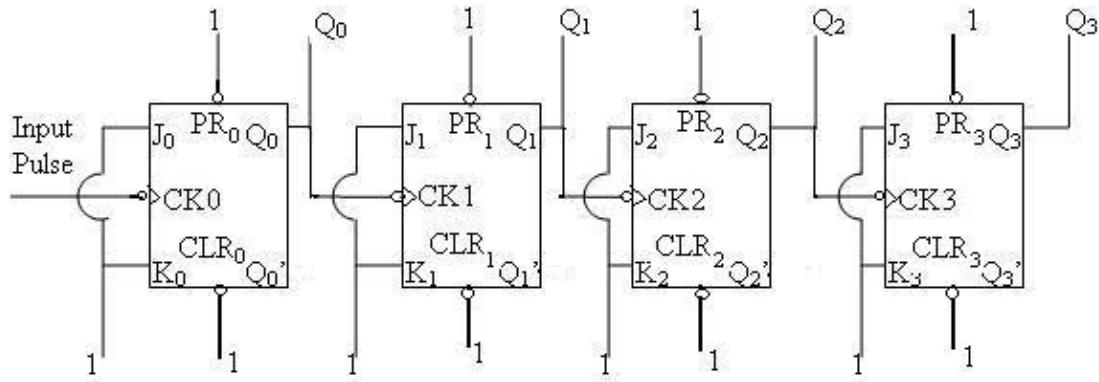
We will consider a basic *4-bit binary up counter*, which belongs to the class of *asynchronous counter* circuits and is commonly known as a *ripple counter*. Since a flip-flop has two states, a counter having n flip-flops will have 2^n states. Hence, in this case the counter will have 2^4 or 16 states.

The schematics below shows a 4-bit up-counter implemented with four JK flip-flops. It can be noticed that the normal output of each flip-flop is connected to the clock input of next flip-flop. Please recall that in case of JK flip-flop, with $J=K=1$, if an input clock pulse is supplied, the output toggles during the positive or negative (which is the

case here, i.e. transition of pulse from 1 to 0) edge of the pulse. The count held by this counter is read in the reverse order from the order in which the flip-flops are triggered. Thus, output Q_3 is the highest order of the count, while output Q_0 is the lowest order. The binary count held by the counter is then $Q = Q_3Q_2Q_1Q_0$.

Let us start from the reset condition of all the flip-flops so that counter reads 0000 (decimal 0). When the trailing or negative end of the first pulse arrives, the first flip-flop gives an output $Q_0=1$, which does not affect the second flip-flop and the counter reads 0001. The counting sequence corresponding to each input pulse is summarized in the table below. On supplying 15th pulse the counter reads 1111 (decimal 15). The next clock pulse after count 1111 will cause the counter to try to increment to 10000 (decimal 16). However, that 1 bit is not held by any flip-flop and is therefore lost. As a result, the counter actually reverts to 0000, and the count begins again.

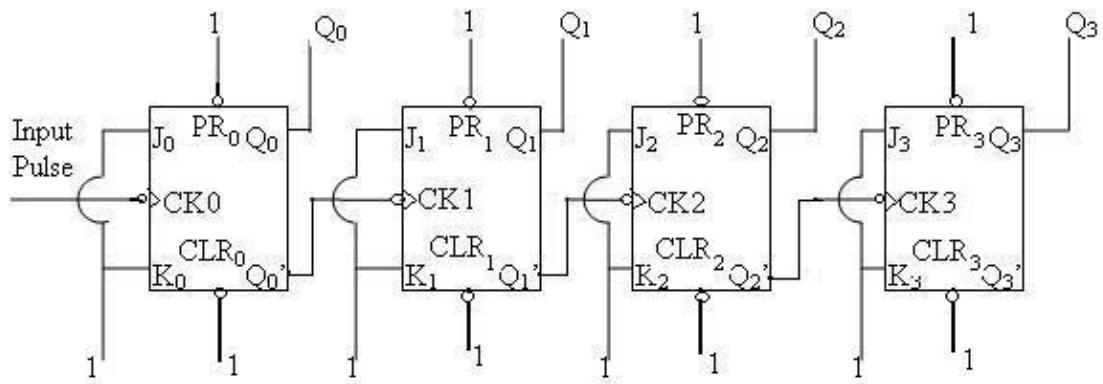
Circuit Diagram:



Binary ripple Down-counter:

The binary ripple down-counter decreases the count by one each time a pulse occurs at the input. The only difference it has from the up-counter is that the complement output of one flip-flop is connected to the clock input of the subsequent flip-flop. Here the complement output toggles at each negative edge of the clock pulse (1 to 0 transition), which is equivalent to a normal output toggling for positive edge of the clock pulse (0 to 1 transition). The counter starts from 1111 with the first pulse after it is reset and reverts back to 0000 after 15 pulses.

Circuit diagram:



Characteristic Tables:

UP COUNTER

DOWN COUNTER

| Input pulse | Binary count | | | | Decimal count |
|-------------|----------------|----------------|----------------|----------------|---------------|
| | Q_3 2^3 | Q_2 2^2 | Q_1 2^1 | Q_0 2^0 | |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 2 |
| 3 | 0 | 0 | 1 | 1 | 3 |
| 4 | 0 | 1 | 0 | 0 | 4 |
| 5 | 0 | 1 | 0 | 1 | 5 |
| 6 | 0 | 1 | 1 | 0 | 6 |
| 7 | 0 | 1 | 1 | 1 | 7 |
| 8 | 1 | 0 | 0 | 0 | 8 |
| 9 | 1 | 0 | 0 | 1 | 9 |
| 10 | 1 | 0 | 1 | 0 | 10 |
| 11 | 1 | 0 | 1 | 1 | 11 |
| 12 | 1 | 1 | 0 | 0 | 12 |
| 13 | 1 | 1 | 0 | 1 | 13 |
| 14 | 1 | 1 | 1 | 0 | 14 |
| 15 | 1 | 1 | 1 | 1 | 15 |
| 16 | 0 | 0 | 0 | 0 | 0 (RESET) |

| Input pulse | Binary count | | | | Decimal count |
|-------------|----------------|----------------|----------------|----------------|---------------|
| | Q_3 2^3 | Q_2 2^2 | Q_1 2^1 | Q_0 2^0 | |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 15 |
| 2 | 1 | 1 | 1 | 0 | 14 |
| 3 | 1 | 1 | 0 | 1 | 13 |
| 4 | 1 | 1 | 0 | 0 | 12 |
| 5 | 1 | 0 | 1 | 1 | 11 |
| 6 | 1 | 0 | 1 | 0 | 10 |
| 7 | 1 | 0 | 0 | 1 | 9 |
| 8 | 1 | 0 | 0 | 0 | 8 |
| 9 | 0 | 1 | 1 | 1 | 7 |
| 10 | 0 | 1 | 1 | 0 | 6 |
| 11 | 0 | 1 | 0 | 1 | 5 |
| 12 | 0 | 1 | 0 | 0 | 4 |
| 13 | 0 | 0 | 1 | 1 | 3 |
| 14 | 0 | 0 | 1 | 0 | 2 |
| 15 | 0 | 0 | 0 | 1 | 1 |
| 16 | 0 | 0 | 0 | 0 | 0 (RESET) |

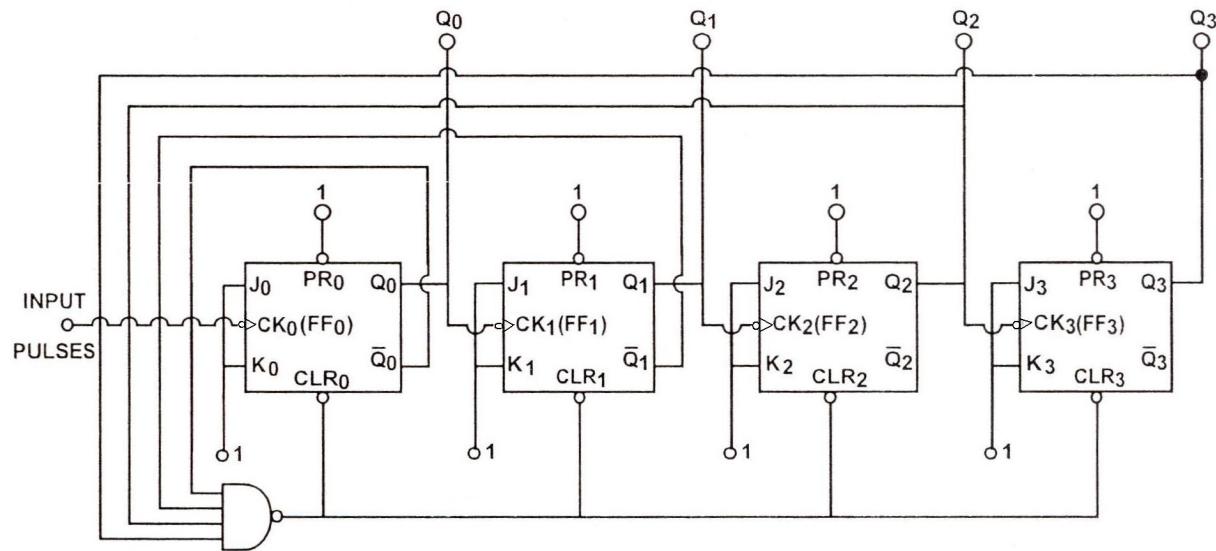
Modulus-12 Counters:

The modulus of a counter is the number of discrete states a counter can take up. A counter with n no. of flip flops will have 2^n number of possible states. So counters with modulus, for example, 2, 4, 8, 16, can be built up using 1, 2, 3, 4 flip flops. It is quite

often desirable to construct a counter having a modulus of 5, 9 or 12 etc. To design counters of modulus-12 (say), one has to use a modulus 16 counter and to arrange the circuit in such a way that it skips some of its natural states restricting it to 12. The simplest way of doing this is the direct clearing method, where a gate circuit is used to clear all the flip flops as the desired count is reached. Thus, for a modulus N counter, the number n of flip-flops should be such that n is the smallest number for which $2^n > N$ and then to skip the surplus states with some rearrangements of the circuit.

The circuit diagram for a Mod-12 counter is shown below. It is obvious that a mod-12 counter will require 4 flip-flops which when connected as a counter, will provide 16 states. This counter counts 0, 1, 2, .., 15 and then it resets to 0. For a mod-12 counter, one may skip state 12 and return to state 0 from state 11 and the cycle should continue this way. For this an additional combinational logic circuit, i.e. a 4-input NAND gate is required, whose output is connected to clear terminal of all the flip flops. This will feed a reset pulse to the counter during state 12 (1100) and immediately after state 11 (1011). The flip-flops are reset and the counter starts counting again.

Circuit diagram:



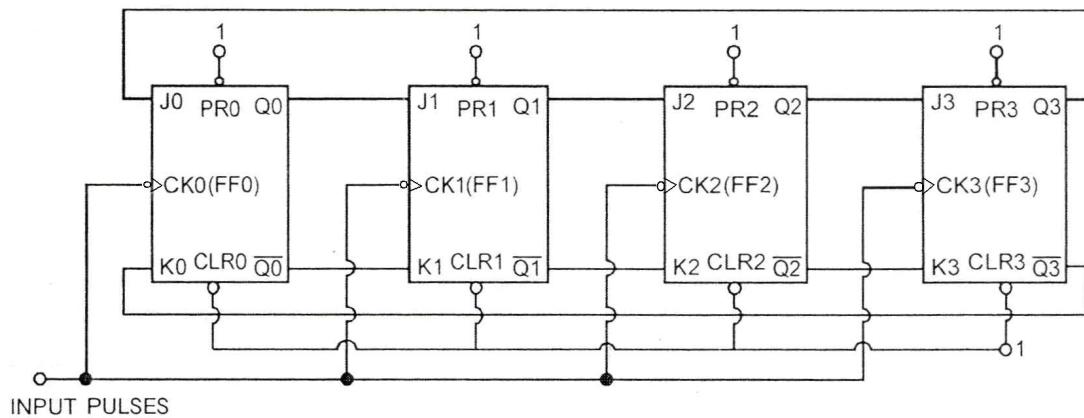
Ring Counter:

Ring counters provide a sequence of equally spaced timing pulses and hence find considerable application in logic circuits which require such pulses for setting in motion a series of operations in a predetermined sequence at precise time intervals. A ring counter consists of an array of coupled flip-flops and the last flip-flop is coupled back to the first as shown in the circuit diagram. If one of the flip-flops is in the SET (or 1) state and the

others are in the RESET (or 0 state) and then applying clock pulses, the logic 1 will advance by one flip-flop around the ring for each pulse. The sequence of operation of the ring counter is summarized in the characteristic table. The logic 1 will return to the original flip-flop after exactly 4 clock pulses (shown in shades) for a 4-bit ring counter.

Ring counter is extremely fast but it is uneconomical in the number of flip-flops (A simple mod-8 counter requires 4 flip-flops whereas a mod-8 ring counter needs 8!!). This is overcome by a modified circuit known as a Johnson counter or switchtail ring counter or twisted counter, where the outputs of the last flip-flop are crossed over and then fed back to the first flip-flop. That is the normal and complement output of the last flip-flop are connected to the K and J inputs of the first flip-flop respectively.

Circuit diagram:



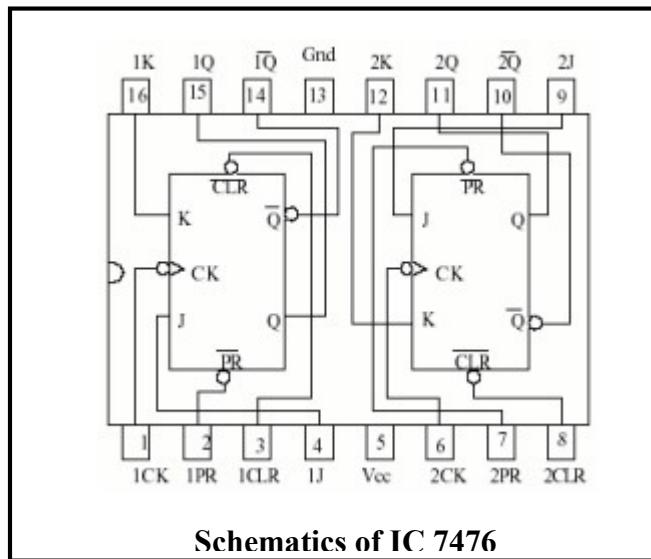
Characteristic Table:

| No. of Input pulses | Binary states | | | |
|---------------------------|----------------|----------------|----------------|----------------|
| | Q ₃ | Q ₂ | Q ₁ | Q ₀ |
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 0 | 0 | 0 |
| 4 | 0 | 0 | 0 | 1 |
| 5 | 0 | 0 | 1 | 0 |
| 6 | 0 | 1 | 0 | 0 |
| 7 | 1 | 0 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 |

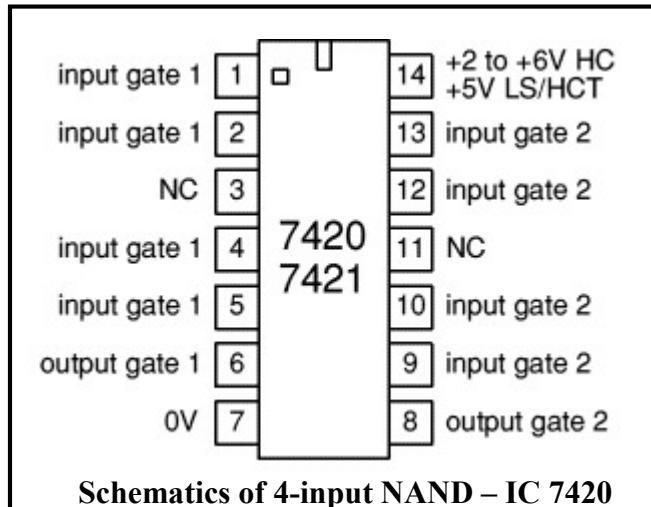
Circuit components/Equipments:

1. Resistors (1KΩ, 5 Nos)
2. ICs [JK FF-7476, 2 Nos; OR-7432,1 No; 2-input AND- 7408, 2 Nos; 4-input NAND -7420, 1 No; NOT-7404, 1 No]
3. A Surface mount dip switch
4. D.C. Power supply (5V)
5. Function Generator
6. Oscilloscope
7. Red/Green LEDs (4 Nos)
8. Connecting wires
9. Breadboard

Circuit Diagrams: Already provided with text.



Schematics of IC 7476



Schematics of 4-input NAND – IC 7420

Procedure:

1. Assemble the circuits one after another on your breadboard as per the circuit diagrams. Circuit diagrams given here do not show connections to power supply and LEDs assuming that you are already familiar with it from your previous lab experience. Here, all the LEDs are connected to the normal output of each flip flop. You will also use the oscilloscope to compare the timing diagrams of each of the output terminal and the input.
2. Connect the ICs properly to power supply and ground following the schematics for ICs given above.
3. Using dip switch and resistors, facilitate the required inputs from the power supply to the J, K, Pr and Cr terminals of the IC.
4. Use the function generator to facilitate clock pulse input to the circuit.
5. Turn on power to your experimental circuit.
6. **Reset** the circuit before applying pulse. **For ring counter preset the first flip-flop to give 1 at its normal output before applying pulse. After verifying it try other combinations.**
7. Set the function generator in “Pulse” mode by pressing the “Function” button. Set the frequency at a very low value (~ 1 Hz, amplitude $\sim 5V$) so that you can notice the logic states of the normal outputs indicated by the LEDs (ON = 1; OFF = 0).
8. The logic states of the J, K inputs must not be allowed to change when clock is high.
9. Record the normal output states of all the flip flops in a table for every pulse applied. Determine characteristic table for each operation.
10. **Feed the input and each of the output of the up-counter to oscilloscope.** Save the waveforms (Timing diagram) and compare their frequencies.
11. When you are done, turn off the power to your experimental circuit.

Observations:

Table for ripple Up-counter: _____

Timing Diagram for up-counter: _____

Table for ripple Down-counter: _____

Table for Mod-12 counter: _____

Table for ring counter : _____

Discussions:

Precautions:

1. Watch out for loose connections.
2. The logic states of the J, K inputs must not be allowed to change when clock is high.

Appendix: IC 7476 datasheet

| Inputs | | | | | Outputs | |
|--------|-----|----------------------|---|---|----------|-------------|
| PR | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H | H |
| | | | | | (Note 1) | (Note 1) |
| H | H | $\uparrow\downarrow$ | L | L | Q_0 | \bar{Q}_0 |
| H | H | $\uparrow\downarrow$ | H | L | H | L |
| H | H | $\uparrow\downarrow$ | L | H | L | H |
| H | H | $\uparrow\downarrow$ | H | H | Toggle | |

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

$\uparrow\downarrow$ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Lab#9: Design and study of IC 555 multivibrator circuits (2 turns)

Objectives:

To design and study the following circuits using IC 555:

- I. An astable multivibrator
- II. A monostable multivibrator
- III. A bistable multivibrator

Overview:

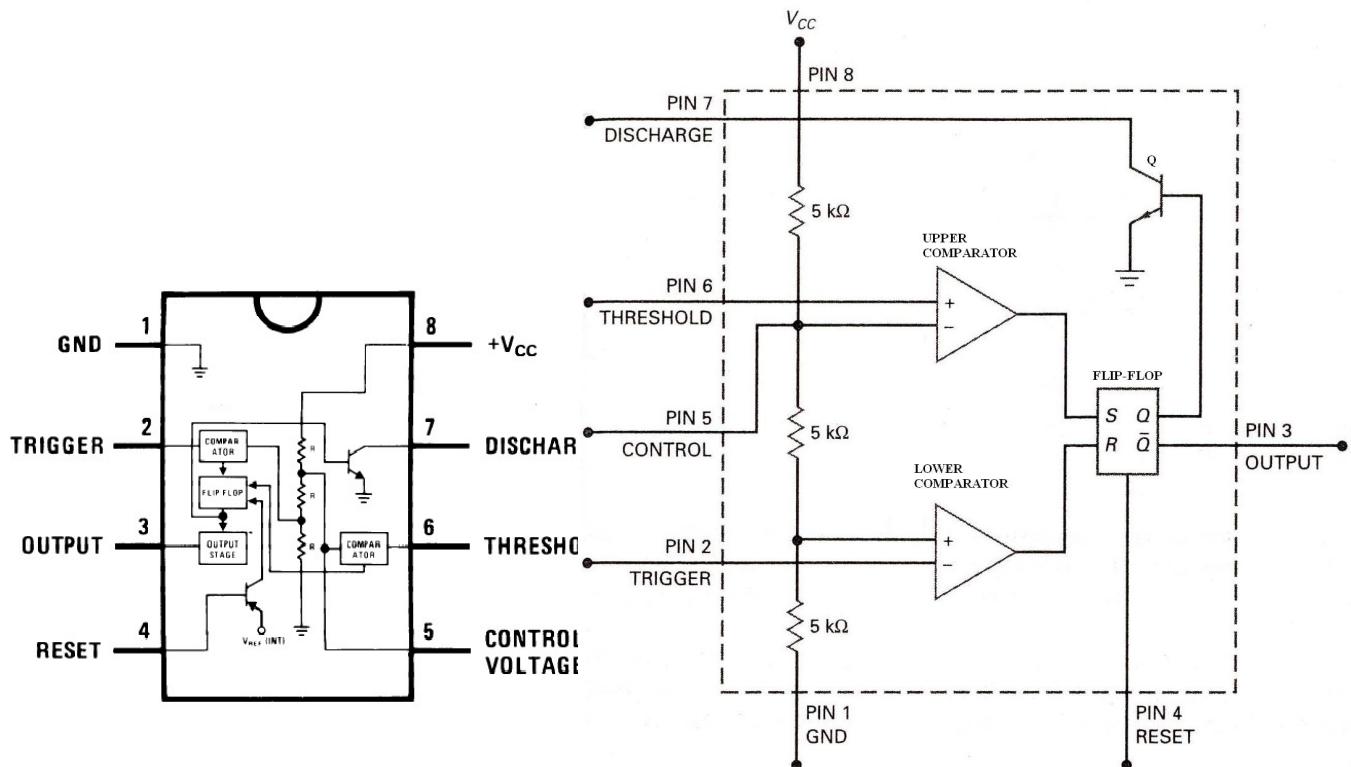
Multivibrators

Individual **Sequential Logic** circuits can be used to build more complex circuits such as Counters, Shift Registers, Latches or Memories etc, but for these types of circuits to operate in a "Sequential" way, they require the addition of a clock pulse or timing signal to cause them to change their state. **Clock pulses** are generally square shaped waves that are produced by a single pulse generator circuit such as a **Multivibrator** which oscillates between a "HIGH" and a "LOW" state and generally has an even 50% duty cycle, that is it has a 50% "ON" time and a 50% "OFF" time. Sequential logic circuits that use the clock signal for synchronization may also change their state on either the rising or falling edge, or both of the actual clock signal. There are basically three types of pulse generation circuits depending on the number of stable states,

- Astable - has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.
- Monostable - has only **ONE** stable state and if triggered externally, it returns back to its first stable state.
- Bistable - has **TWO** stable states that produces a single pulse either positive or negative in value.

IC 555 TIMER

The 555 timer IC was first introduced around 1971 by the Signetics Corporation as the SE555/NE555 and was called "**The IC Time Machine**" and was also the very first and only commercial timer IC available. It provided circuit designers with a relatively cheap, stable, and user-friendly integrated circuit for timer and multivibrator applications. These ICs come in two packages, either the round metal-can called the 'T' package or the more familiar 8-pin DIP 'V' package as shown in figure below. The IC comprises of 23 transistors, 2 diodes and 16 resistors with built-in compensation for component tolerance and temperature drift.



IC 555 in 8-pin DIP package

Functional block diagram of IC 555

The pin connections are as follows:

1. Ground.
2. Trigger input.
3. Output.
4. Reset input.
5. Control voltage.
6. Threshold input.
7. Discharge.
8. $+V_{CC}$. +5 to +15 volts in normal use.

Pin1: Ground. All voltages are measured with respect to this terminal.

Pin2: Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. When a negative going pulse of amplitude greater than $1/3 V_{CC}$ is applied to this pin, the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin3: Output. The output of the timer is measured here with respect to ground. There are two ways by which a load can be connected to the output terminal: either between pin 3 and ground or between pin 3 and supply voltage $+V_{CC}$. When the output is low the load current flows through the load connected between pin 3 and $+V_{CC}$ into the output terminal and is called sink current. The current through the grounded load is zero when the output is low. For this reason the load connected between pin 3 and $+V_{CC}$ is called the *normally on load* (we will use this for our circuit) and that connected between pin 3 and ground is called *normally off-load*. On the other hand, when the output is high the current through the load connected between pin 3 and $+V_{CC}$ is zero. The output terminal supplies current

to the normally off load. This current is called source current. The maximum value of sink or source current is 200mA.

Pin4: Reset. The 555 timer can be reset (*disabled*) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{CC}$ to avoid any possibility of false triggering.

Pin5: Control Voltage. An external voltage applied to this terminal changes the threshold as well as trigger voltage. Thus by imposing a voltage on this pin or by connecting a *pot* between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a $0.01\mu F$ Capacitor to prevent any noise problems.

Pin6: Threshold. When the voltage at this pin is greater than or equal to the threshold voltage $2/3 V_{CC}$, the output of the timer low.

Pin7: Discharge. This pin is connected internally to the collector of transistor Q. When the output is high Q is OFF and acts as an open circuit to external capacitor C connected across it. On the other hand, when the output is low, Q is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin8: $+V_{CC}$. The supply voltage of $+5V$ to $+18V$ is applied to this pin with respect to ground.

OPERATION:

The functional block diagram shows that the device consists of two comparators, three resistors and a flip-flop. A comparator is an OPAMP that compares an input voltage and indicates whether an input is higher or lower than a reference voltage by swinging into saturation in both the direction. The operation of the 555 timer revolves around the three resistors that form a voltage divider across the power supply to develop the reference voltage, and the two comparators connected to this voltage divider. The IC is quiescent so long as the trigger input (pin 2) remains at $+V_{CC}$ and the threshold input (pin 6) is at ground. Assume the reset input (pin 4) is also at $+V_{CC}$ and therefore inactive, and that the control voltage input (pin 5) is unconnected.

The three resistors in the voltage divider all have the same value (5K in the bipolar version of this IC and hence the name 555), so the trigger and threshold comparator reference voltages are $1/3$ and $2/3$ of the supply voltage, respectively. The control voltage input at pin 5 can directly affect this relationship, although most of the time this pin is unused. The internal flip-flop changes state when the trigger input at pin 2 is pulled down below $+V_{CC}/3$. When this occurs, the output (pin 3) changes state to $+V_{CC}$ and the discharge transistor (pin 7) is turned off. The trigger input can now return to $+V_{CC}$; it will not affect the state of the IC.

However, if the threshold input (pin 6) is now raised above $+(2/3)V_{CC}$, the output will return to ground and the discharge transistor will be turned on again. When the threshold input returns to ground, the IC will remain in this state, which was the original state when we started this analysis. The easiest way to allow the threshold voltage (pin 6) to gradually rise to $+(2/3)V_{CC}$ is to connect it externally to a capacitor being allowed to charge through a resistor. In this way we can adjust the R and C values for almost any time interval we might want.

IC 555 Timer as Multivibrator

The 555 can operate in either mono/bi-stable or astable mode, depending on the connections to and the arrangement of the external components. Thus, it can either produce a single pulse when triggered, or it can produce a continuous pulse train as long as it remains powered.

Astable multivibrator

These circuits are not stable in any state and switch outputs after predetermined time periods. The result of this is that the output is a continuous square/rectangular wave with the properties depending on values of external resistors and capacitors. Thus, while designing these circuits following parameters need to be determined:

1. Frequency (or the time period) of the wave.
2. The duty cycle of the wave.

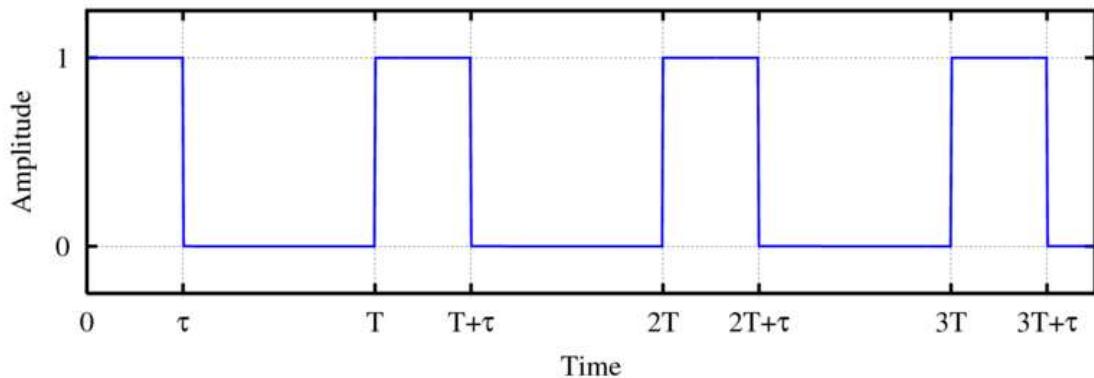


Figure 1: A rectangular waveform

Referring to the above figure of a rectangular waveform, the time period of the pulse is defined as T and duration of the pulse (ON time) is τ . Duty cycle can be defined as the On time/Period that is, τ/T in the above figure. Obviously, a duty cycle of 50% will yield a square wave.

The key external component of the **astable timer** is the *capacitor*. An astable multivibrator can be designed as shown in the circuit diagram (with typical component values) using IC 555, for a duty cycle of more than 50%. The corresponding voltage across the capacitor and voltage at output is also shown. The astable function is achieved by charging/discharging a capacitor through resistors connected, respectively, either to V_{CC} or GND. Switching between the charging and discharging modes is handled by

resistor divider R_1-R_3 , two Comparators, and an RS Flip-Flop in IC 555. The upper or lower comparator simply generates a positive pulse if V_C goes above $2/3 V_{CC}$ or below $1/3 V_{CC}$. And these positive pulses either SET or RESET the Q output.

The time for charging C from $1/3$ to $2/3 V_{CC}$, i.e. **ON Time = $0.693 \cdot (R_A + R_B) \cdot C$**

The time for discharging C from $2/3$ to $1/3 V_{CC}$, i.e. **OFF Time = $0.693 \cdot R_B \cdot C$**

To get the total oscillation period, just add the two:

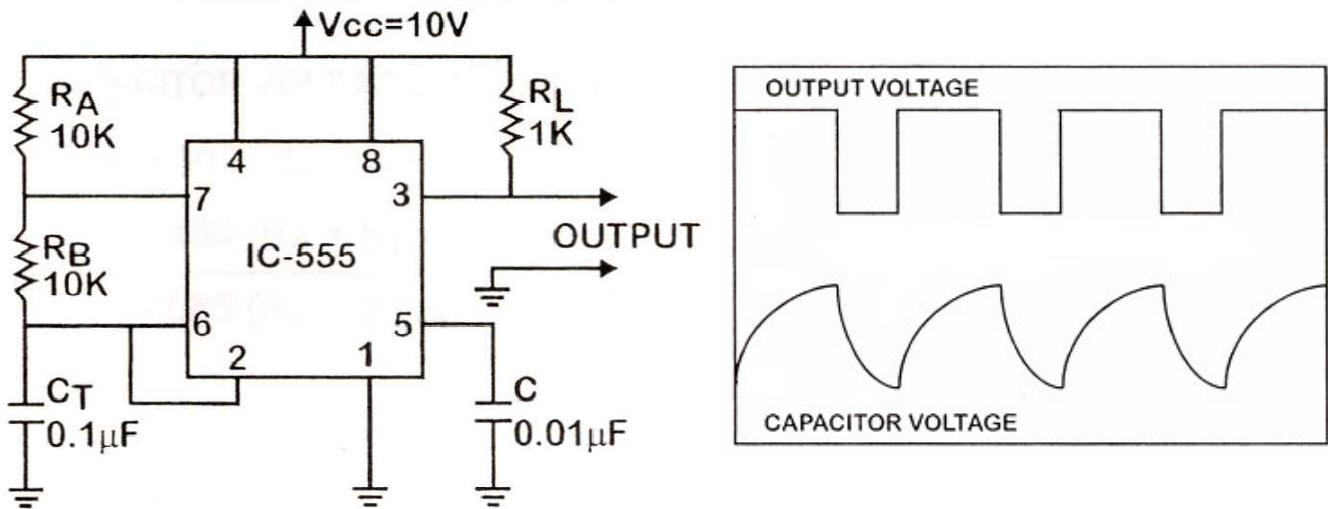
$$T_{osc} = 0.693 \cdot (R_A + R_B) \cdot C + 0.693 \cdot R_B \cdot C = 0.693 \cdot (R_A + 2 \cdot R_B) \cdot C$$

Thus,

$$f_{osc} = 1/T_{osc} = 1.44 / (R_A + 2 \cdot R_B) \cdot C$$

$$\text{Duty cycle} = R_A + R_B / (R_A + 2 \cdot R_B)$$

Circuit Diagram:



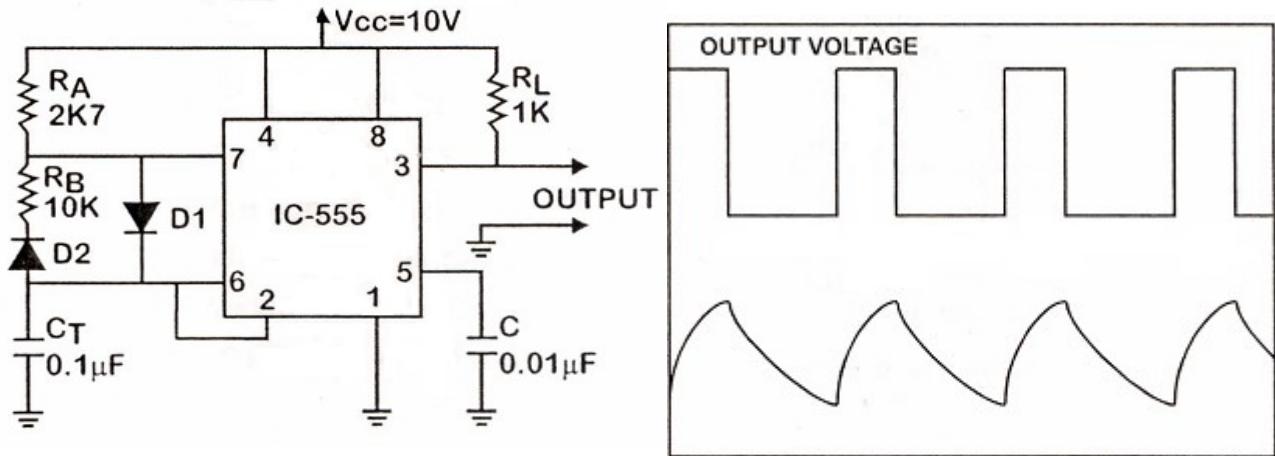
Astable multivibrator with duty cycle less than 50%:

Generally astable mode of IC 555 is used to obtain the duty cycle between 50 to 100%. But for a duty cycle less than 50%, the circuit can be modified as per the circuit diagram. Here a diode D1 is connected between the discharge and threshold terminals (as also across R_B). Thus the capacitor now charges only through R_A (since R_B is shorted by diode conduction during charging) and discharges through R_B . Another optional diode D2 is also connected in series with R_B in reverse direction for better shorting of R_B . Therefore, the frequency of oscillation and duty cycle are

$$f_{osc} = 1/T_{osc} = 1.44 / (R_A + R_B) \cdot C$$

$$\text{Duty Cycle} = R_A / (R_A + R_B)$$

Circuit Diagram:



Astable multivibrator with duty cycle variable from 0 to 100%:

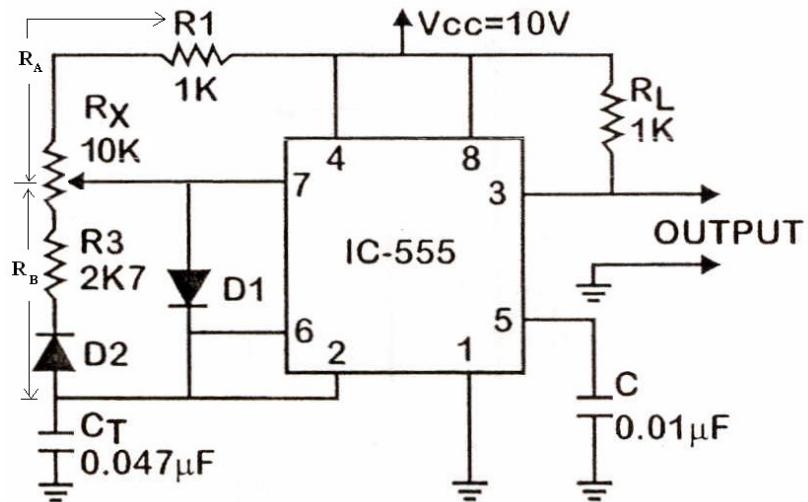
In some applications, it is needed to vary the duty cycle from about 0 to 100%. In that case the circuit is designed as shown in the circuit diagram. Here a potentiometer, R_X , is used so that $R_A = R_1 + R_2$, $R_B = R_X - R_2 + R_3$. A diode is now connected across a variable R_B . Thus a variable duty cycle is achieved. Therefore, the frequency of oscillation and duty cycle can be derived as follows.

$$f_{osc} = 1/T_{osc} = 1.44/(R_A + R_B) \cdot C = 1.44/(R_1 + R_X + R_3) \cdot C$$

$$\text{Min. Duty Cycle} = R_1/(R_1 + R_X + R_3)$$

$$\text{Max. Duty Cycle} = (R_1 + R_X)/(R_1 + R_X + R_3)$$

Circuit Diagram:



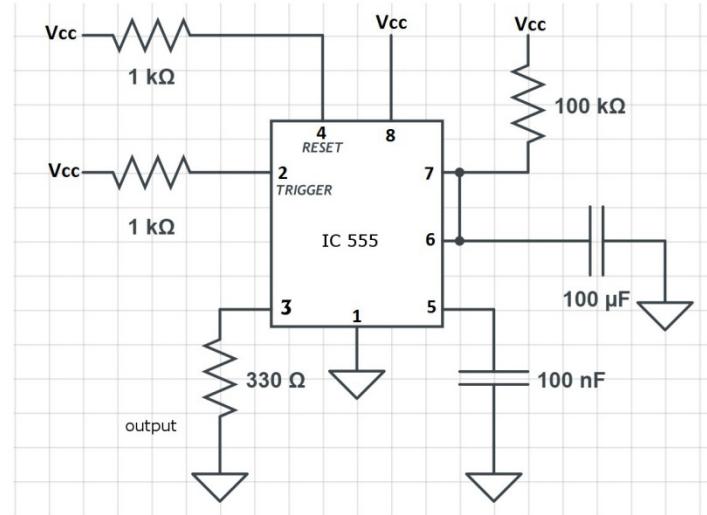
Monostable multivibrator

Monostable multivibrator often called a *one shot* multivibrator is a pulse generating circuit in which the duration of this pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state, the output of the circuit is approximately zero or a logic-low level. When external trigger is applied (See circuit diagram) output is forced to go high ($\approx V_{CC}$). The time for which output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (*output low*) hence the name *monostable*.

Initially when the circuit is in the stable state i.e, when the output is low, transistor Q in IC 555 is ON and the capacitor C is shorted out to ground. Upon the application of a negative trigger pulse to pin 2, transistor Q is turned OFF, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{CC} through R. When the voltage across the capacitor equals $2/3 V_{CC}$, the upper comparator's (see schematics of IC 555) output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time the output of the flip-flop turns transistor Q ON and hence the capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. The pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative going input signal with amplitude larger than $1/3 V_{CC}$ (Why?). The pulse width can be calculated as (How?): **T= 1.1 R.C.**

Once triggered, the circuit's output will remain in the high state until the set time, T, elapses. The output will not change its state even if an input trigger is applied again during this time interval. The circuit can be reset during the timing cycle by applying negative pulse to the reset terminal. The output will remain in the low state until a trigger is again applied. The circuit is designed as shown in the circuit diagram, the left part of which shows how to generate negative a trigger pulse from a square wave signal.

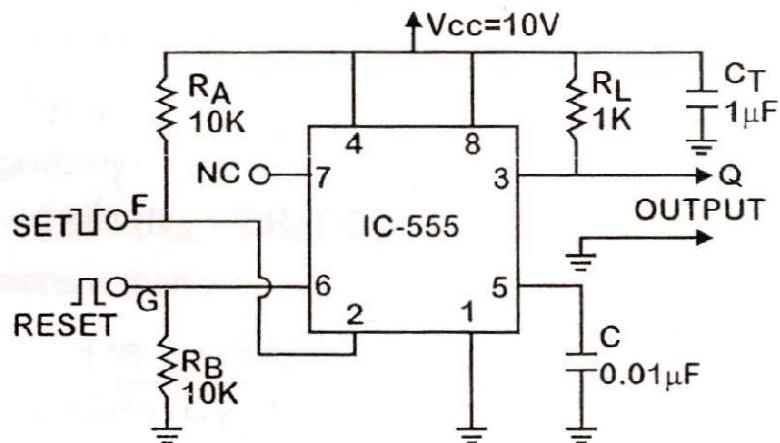
Circuit Diagram:



Bistable Multivibrator

In these circuits, the output is stable in both the states. The states are switched using an external trigger but unlike the monostable multivibrator, it does not return back to its original state. Another trigger is needed for this to happen. This operation is similar to a flip-flop. There are no RC timing network and hence no design parameters. The following circuit can be used to design a bistable multivibrator. The trigger and reset inputs (pins 2 and 4 respectively on a 555) are held high via pull-up resistors while the threshold input (pin 6) is simply grounded. Thus configured, pulling the trigger momentarily to ground acts as a 'set' and transitions the output pin (pin 3) to Vcc (high state). Pulling the threshold input to supply acts as a 'reset' and transitions the output pin to ground (low state). No capacitors are required in a bistable configuration.

Circuit Diagram:



Circuit components/Equipments:

1. IC 555 (1 No.)
2. Resistors (1K Ω , 2 Nos; 10K Ω , 2 Nos; 2.7K Ω , 1 No)
3. Potentiometer (10 K Ω , 1 No)
4. Capacitors (0.01 μ F, 0.047 μ F, 0.1 μ F, 1 μ F; 1 No. each)
5. Diodes 1N 4148 (2 Nos.)
6. D.C. Power supply (10V)
7. Function Generators
8. Oscilloscope
9. Connecting wires
10. Breadboard

Circuit Diagrams: Already provided with text.

Procedure:

I. Astable Multivibrator:

(a) For duty cycle more than 50%:

1. Configure the circuit as per the circuit diagram.
2. Use $R_A = R_B = 10 \text{ k}\Omega$, $R_L = 1 \text{ k}\Omega$ and $C_T = 0.1 \mu\text{F}$, $C = 0.01 \mu\text{F}$. Using the power supply set $V_{CC} = 10 \text{ V}$.
3. Compute the expected values of f_{osc} and duty cycle (%).
4. Connect the output terminal (pin 3) to channel 1 of the oscilloscope. Also feed the voltage across capacitor to channel 2.
5. Power on your circuit and observe and save the output. Determine the values of f_{osc} and duty cycle (%) from your observations and compare with the theoretical values.
6. When you are done, turn off the power to your experimental circuit.

(b) For duty cycle less than 50%:

1. Configure the circuit as per the circuit diagram.
2. Use $R_A = 2.7 \text{ k}\Omega$, $R_B = 10 \text{ k}\Omega$, $R_L = 1 \text{ k}\Omega$ and $C_T = 0.1 \mu\text{F}$, $C = 0.01 \mu\text{F}$. Using the power supply set $V_{CC} = 10 \text{ V}$.
3. Repeat steps 3 to 6 of procedure (a).

(c) For duty cycle variable from 0 to 100%:

1. Configure the circuit as per the circuit diagram.
2. Use $R_1 = 1 \text{ k}\Omega$, $R_2 = 2.7 \text{ k}\Omega$, $R_X = 10 \text{ k}\Omega$, $R_L = 1 \text{ k}\Omega$ and $C_T = 0.047 \mu\text{F}$, $C = 0.01 \mu\text{F}$. Using the power supply set $V_{CC} = 10 \text{ V}$.
3. Calculate R_A and R_B for different settings of the potentiometer using $R_A = R_1 + R_2$, $R_B = R_X - R_2 + R_3$ and repeat steps 3 to 6 of procedure (a) for each setting.

II. Monostable Multivibrator

1. Configure the circuit as per the circuit diagram. set $V_{CC} = 10 \text{ V}$
2. Connect the output terminal (pin 3) to the oscilloscope.

3. Power on your circuit and trigger the circuit using momentarily connecting jumper wire from 2 to ground and observe the output.
4. Observe time for which output is high, compare with RC value. While output is high, try triggering repeatedly and observe the output.

III. Bistable Multivibrator

1. Configure the circuit as per the circuit diagram.
2. Use $R_A = R_B = 10 \text{ k}\Omega$, $R_L = 1 \text{ k}\Omega$ and $C_1 = 1 \mu\text{F}$, $C_2 = 0.01 \mu\text{F}$. Using the power supply set $V_{CC} = 10 \text{ V}$.
3. Connect the output terminal (pin 3) to the oscilloscope in **DC COUPLING** mode.
4. Power on your circuit.
5. Connect the point F to ground momentarily. This will set the output Q in the oscilloscope to 1 or HIGH level. This state will be permanently stable state and the operation is called “SET”.
6. Now connect the point G to V_{CC} momentarily. This will set the output Q in the oscilloscope to 0 or LOW level. This is called “RESET” operation.
7. When you are done, turn off the power to your experimental circuit

Observations:

I. Astable Multivibrator:

(a) For duty cycle more than 50%:

$$R_A = R_B = \text{_____} \text{ k}\Omega, C_T = \text{_____} \mu\text{F}$$

Output waveform and capacitor voltage as observed in oscilloscope: (paste data here)

| Parameters | Calculated value | Observed value | Error |
|----------------|------------------|----------------|-------|
| f_{osc} | | | |
| Duty cycle (%) | | | |

(b) For duty cycle more than 50%:

$$R_A = \text{_____} \text{ k}\Omega, R_B = \text{_____} \text{ k}\Omega, C_T = \text{_____} \mu\text{F}$$

Output waveform and capacitor voltage as observed in oscilloscope: (paste data here)

| Parameters | Calculated value | Observed value | Error |
|----------------|------------------|----------------|-------|
| f_{osc} | | | |
| Duty cycle (%) | | | |

(c) For duty cycle variable from 0 to 100%:

$$R_1 = \text{_____} \text{ k}\Omega, R_2 = \text{_____} \text{ k}\Omega, R_X = \text{_____} \text{ k}\Omega, C_T = \text{_____} \mu\text{F}$$

Output waveform and capacitor voltage as observed in oscilloscope: (paste data here for each setting of the pot.)

Calculated $f_{osc} = \underline{\hspace{2cm}}$

| Sl. No. | $R_A(k\Omega)$ | $R_B(k\Omega)$ | Observed f_{osc} (kHz) | Duty cycle (%) | | Error |
|---------|----------------|----------------|-----------------------------|----------------|------------|-------|
| | | | | Observed | Calculated | |
| 1 | $R_1 = ..$ | | | Minimum = .. | | |
| .. | | | | | | |
| .. | | | | | | |
| 5 | $R_1 + R_X$ | | | Maximum = .. | | |

II. Monostable Multivibrator:

$$R_A = \underline{\hspace{2cm}} \text{ k}\Omega, C_T = \underline{\hspace{2cm}} \mu\text{F}$$

| Parameter | Calculated value (ms) | Observed value (ms) | Error |
|----------------------|--------------------------|------------------------|-------|
| Output high duration | | | |

III. Bistable Multivibrator:

| Point | Connected to | Output |
|-------|--------------|--------|
| F | Ground | |
| G | V_{CC} | |

Discussions:

Precautions:
